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NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

DESIGN OF A SATELLITE-BASED MICROELECTRONIC RADIATION TESTING EXPERIMENT

by

Christopher S. Mooney

March 1996

Thesis Advisor: Douglas Fouts

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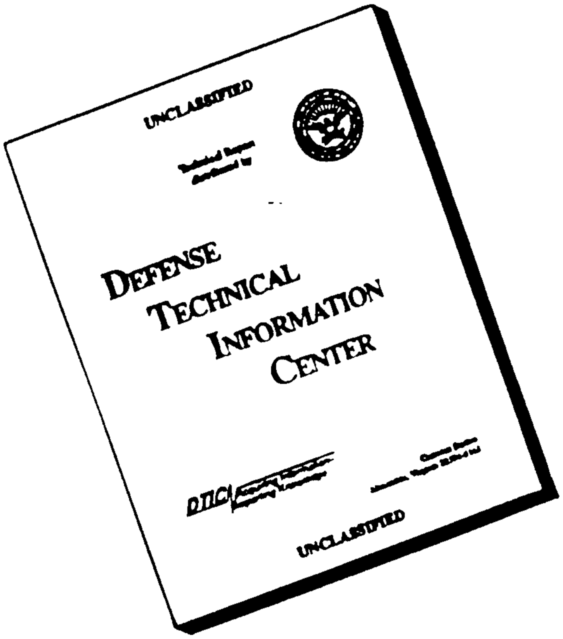

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DESIGN OF A SATELLITE-BASED MICROELECTRONIC RADIATION TESTING EXPERIMENT

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requirements for the degree of

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ABSTRACT

In this research, an electronic daughterboard to be used on the Microelectronics and Photonics Test Bed satellite was designed. A printed circuit board with radiation-hardened components was laid out to test various families of static RAM chips and an experimental Gallium-Arsenide integrated circuit. Computer-aided-design tools produced by Cadence Design Systems were used to logically and physically design the experiment. Output from the Cadence software provides the information necessary to fabricate, assemble, and test the board.

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I. INTRODUCTION

A. OVERVIEW

In order to understand the effects of space radiation on several different new electronic and opto-electronic technologies, the Department of Defense (DoD) has scheduled a satellite launch to study the new devices. The satellite, the Microelectronics and Photonics Test Bed (MPTB), is a satellite payload that will be used to measure the effects of space radiation on microelectronic and photonic devices and subsystems. Changes in device characteristics caused by space radiation will be measured in a controlled experiment. Total Ionizing Dose (TID), Dose-Rate Effects (DRE), and Single Event Upsets (SEU) are phenomenon to be studied in the MPTB experiment. Experimental results will be transmitted to ground stations for further analysis and dissemination.

This thesis documents the design of an experiment to test for memory errors caused from TID, DRE and SEU on high-speed integrated circuit (IC) memory chips of various logic families. The design contains a microcontroller to write test patterns to each memory chip and then monitor the integrity of the data. Detected errors will then be compiled and recorded. Addditionally, the experiment will be designed to control an experimental GaAs IC. The chip autonomously writes, tests, and compiles its own test data, but requires input to start and set internal clock speed. Finally, the output data of the experiment must be sent to the main control unit of the MPTB in order to be transmitted to a ground station.

B. THESIS ORGANIZATION

The goal of this thesis is to design a printed circuit board (PCB) with radiation-hardened components in order to test orbital radiation effects of the selected test chips and to relay this information to the main control package of the MPTB. Chapter II will present an overview of the radioactive environment of space and how this impacts semiconductor components. Chapter III discusses the MPTB satellite and daughterboard interfacing to the satellite. Chapter IV will discuss component selection and issues concerned with using the components together. Chapter V discusses connectivity and operation of the designed PCB. Chapter VI presents a summary of the Cadence Board Design tools. Chapter VII presents conclusions, future considerations, and requirements.

II. SATELLITE ENVIRONMENT

A. RADIATION EFFECTS ON SEMICONDUCTORS

1. TIDs, DREs & SEUs

Ionizing radiation effects in space vehicle electronics can be separated into three areas: total ionizing dose (TID), dose-rate effects (DRE), and single event upsets (SEU). Each of these effects are distinct with respect to one another, however, the underlying result of all three effects is the malfunction of electronic components in orbit. Reference 2 contains an in depth summary of these problems. The remainder of this chapter shall point out the important aspects of effects.

TID is the long-term degradation of electronics due to the cumulative energy deposited in a material. Effects include parametric failures or variations in device parameters such as leakage current, threshold voltage, etc., and functional failures. Significant sources of TID exposure in the space environment include trapped electrons, trapped protons, and solar flare protons.

Another negative cumulative effect on semiconductor devices is caused by neutron bombardment. Neutrons and other high mass particles cause displacement damage from physical interaction with the silicon lattice. This damage results in decreased minority carrier capacity, increased junction leakage currents, and reduced carrier mobility. Significant numbers of neutrons are present during solar flare activity.

DREs occur when a short-duration, high energy burst of radiation strikes a semiconductor and induces an electric current in the semiconductors substrate. The induced current is potentially sufficient to be destructive to electronic devices. One example of a DRE is latchup. Modern electronic components make extensive use of complementary field-effect transistors. An unwanted by-product of this technology is the presence of parasitic bipolar-junction transistors (BJT) at the well/substrate PN junction. A high energy burst of radiation can generate the necessary current to "turn-on" the parasitic BJTs. This effectively creates a short-circuit between power and ground, resulting in the disabling or destruction of the associated FET.

SEUs occur when a single ion strikes the material, depositing sufficient energy in the device to cause a fault. SEUs may be divided into two main categories: soft errors and latchup. In general, a soft error occurs when a transient pulse or bit-flip in the device causes a detectable error at the device output. Therefore, soft errors are entirely device specific and are best categorized by

their impact on the device. Latchup may be physically destructive to the device, and can cause permanent or semi-permanent functional problems.

2. Impact of Radiation Effects

Device parametric and permanent functional failure are the principal failure modes associated with the TID environment. Since TID is a cumulative effect, total dose tolerances of devices are characterized as mean-time-to-failure (MTTF), where the time-to-failure is the amount of mission time until the device has encountered enough dose to cause failure. The mission orbit, launch date, and launch length determine the external radiation environment. The device exposure to this hazard is determined by the amount of shielding between the device and the external environment.

The system-level impact of SEU depends on the type and location of the effect, as well as on the design. Permanent device failure is obviously of great concern. The effects of propagation of transient SEUs through a circuit, subsystem, and system are also of particular importance. For example, a device error or failure may have effects propagating to critical mission elements, such as a command error affecting thruster firing. There are also cases where SEUs may have little or no observable effect on a system.

B. SOURCE OF ORBITAL RADIATION

The main sources of radiation that contribute to TID, DRE and SEU are:

- Protons and electrons trapped in the Van Allen belts.
- Cosmic ray protons and heavy ions.
- Neutron, protons and heavy ions from solar flares.

The levels of some of these sources are affected by the activity of the sun. The solar cycle varies from a solar minimum to a solar maximum. An average cycle lasts about 11 $^1/_2$ years. A solar maximum lasts 1 to 2 years and is followed by a 3 to 4 year period of decreasing solar activity after which a solar minimum occurs. A solar minimum lasts 1 to 2 years and is followed by a period of increasing activity of 3 to 4 years.

1. Charged Particles Trapped in the Van Allen Belts

SEUs in high density electronic parts are primarily caused by proton bombardment in the Van Allen Radiation Belt. It is difficult to shield against high energy protons that cause SEU problems and contribute significantly to TID, within the weight budget of a spacecraft. The Van

Allen Radiation Belt is a region around the earth consisting primarily of positively charged protons and negatively charged electrons. The belt is divided into an inner and outer zone. The inner zone begins at a few hundred miles altitude at the equator to approximately 5,600 miles. The outer region extends from 7,200 miles out, to approximately 44,000 miles out [Ref. 3, p.3]. The particle density of the outer zone is higher by about an order of magnitude compared to the inner zone. An area of particular interest is the South America Anomaly (SAA). The SAA is a region of the Van Allen Belt where the lower boundary of the inner zone dips to a mere 50 to 100 nautical miles above the surface of the earth. Thus, even satellites in the lowest orbits are effected. The level of radioactive activity and the actual physical boundaries of the Van Allen Belt depend on particle energy and are affected by secular variation in the magnetic field, magnetic perturbations, local time effects, solar cycle variations, and individual solar events.

2. Cosmic Ray Protons and Heavy Ions

Galactic cosmic ray particles originate outside of the solar system. The flux levels of these particles are low, but because they include highly energetic particles of heavy elements such as iron, they produce intense ionization as they pass through matter. Cosmic ray particle population also varies with the solar cycle. The earths magnetic field provides spacecraft with varying degrees of protection from the cosmic rays, depending primarily on the inclination but also on the altitude of the orbit. The energy levels of galactic cosmic ray particles also vary with the ionization state of the particle

3. Protons, Neutrons, and Heavy Ions from Solar Flares

When solar flare activity is present, high concentrations of protons, neutrons, and heavy ions are present in earth orbit. The level of solar flare activity from the sun varies with the 11 $^1/_2$ year solar cycle. The solar maximum is characterized by solar activity during which large flare events can occur. Events last from several hours to a few days and energies may reach a few hundred MeV. As with the galactic cosmic ray particles, the solar flare particles are attenuated by the magnetosphere of the earth. As with the high energy trapped protons, they are difficult to shield against. Therefore, in spite of their low numbers, they constitute a significant hazard to electronics in terms of SEUs.

4. Variation In Radioactive Exposure

There are extremely large variations in the TID, DRE and SEU levels that a given spacecraft encounters, depending on its orbit through the radiation sources. Low Earth Orbit (LEOs) satellites pass through the particles trapped in the Van Allen belts several times each day, especially in the vicinity of the SAA. The amount of radiation that a satellite is exposed to during these passes varies greatly with orbit inclination and altitude. Highly Elliptical Orbits (HEOs) are similar to LEOs in that they pass through the Van Allen belts each day. However, because of their high altitude, they also have long exposures to the cosmic ray and solar flare environments regardless of their inclination. In Geosynchronous Orbits (GEOs), the only trapped protons that are present are below energy levels necessary to initiate the nuclear events in materials surrounding the sensitive region of the device that cause SEUs. However, GEOs are almost fully exposed to the galactic cosmic ray and solar flare particles.

III. MICROELECTRONICS & PHOTONICS TEST BED SATELLITE

A. DAUGHTERBOARD EXPERIMENT DESIGN

1. Overview

The design project is a daughterboard experiment for the MPTB. The experiment is designed to test high-speed integrated circuit (IC) memory chips in the high radiation environment the MPTB is scheduled to fly in. The daughterboard will perform two primary functions. First, the daughterboard will write test patterns to memory chips, each of a different logic family. The test patterns will be continuously monitored for evidence of SEUs, DREs, and TID. Second, the daughterboard will control an experimental gallium-arsenide (GaAs) IC. Results will be compiled, stored, and sent to the MPTBs Core Electronics Unit for transmission to a ground station.

2. High-Speed Logic

The high-speed logic test is designed to compare memory ICs of different logic families for susceptibility to space radiation. The experiment is not designed to compare the access speeds of the different memory ICs. For the high speed logic experiment, a 256 x 4 gallium-arsenide (GaAs) static random-access memory (SRAM) IC and a 256 x 4 emitter-coupled-logic (ECL) SRAM IC were chosen to test. A 4k x 4 CMOS SRAM IC was added to provide a baseline for comparison.

a. GaAs

Gallium arsenide is the fastest logic technology with gate delays as low as 10 picoseconds [Ref.1, p.970]. GaAs technology utilizes field-effect transistors, but because the mobility of electrons for gallium-arsenide is five times that of silicon, GaAs gates are substantially faster then their silicon counterparts. GaAs ICs also consume considerably less power than CMOS circuits of comparable speed and functionality. Furthermore, it is also less expensive than ECL or BiCMOS, and it the fastest commercially available logic family. On the negative side, this technology suffers from a relatively narrow noise margin.

b. ECL

Emitter coupled logic is the fastest technology based on bipolar junction transistors. Gate delay for this logic is as low as 1 nanosecond [Ref. 4, p.175]. The disadvantages to ECL include high current levels, causing high power dissipation and heat buildup, which is difficult to dissipate. Another negative attribute of ECL is poor IC integration. Voltage levels for

this family are -5.2 and 0 volts for a logical one and zero respectively, making ECL chips compatible with CMOS and TTL only through the use of logic converters.

c. *CMOS*

Complimentary metal oxide (CMOS) semiconductors are by far the most popular family of IC logic. Strengths of this family include very low power dissipation, the capability for very high degrees of integration, and low cost to manufacture. However, silicon FETs do not possess the gate speeds as other logic families.

3. Experimental GaAs IC

The GaAs experimental chip is semi-autonomous. The chip generates its own test patterns at eight different clock speeds, monitors itself for errors, and counts the number of SEUs that occur. The chip does require outside inputs to begin execution, select a clock speed, and latch results.

B. MPTB FUNCTIONAL DESCRIPTION

The MPTB consists of a central Core Electronics Unit (CEU) and three experiment panels. MPTB experiments occupy daughterboard slots on each panel. Up to eight daughterboards may be fitted on each panel. A block diagram is shown in Figure 1.

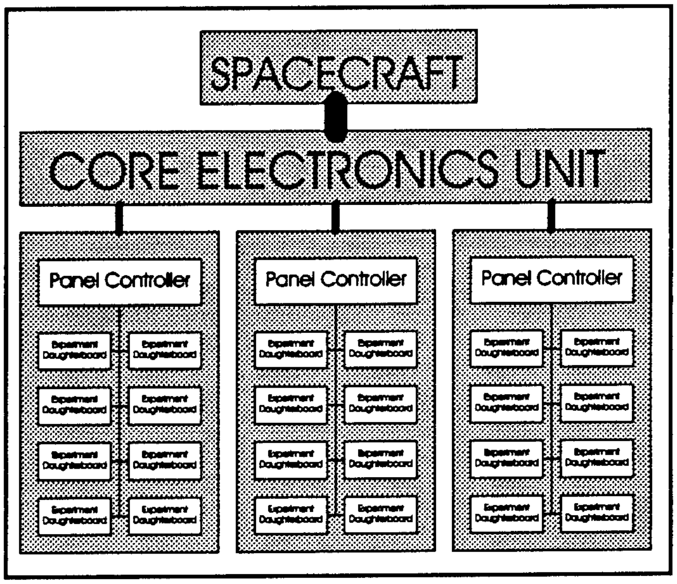

Figure 1: MPTB Functional Layout

C. DAUGHTERBOARD INTERFACE WITH SATELLITE

1. Connectivity

The CEU manages overall operation of the MPTB, including sending telemetry to ground stations. Daughterboard experiments communicate with the CEU via Experimental Panel Controllers (EPC) . Figure 2 shows a block diagram of the EPC.

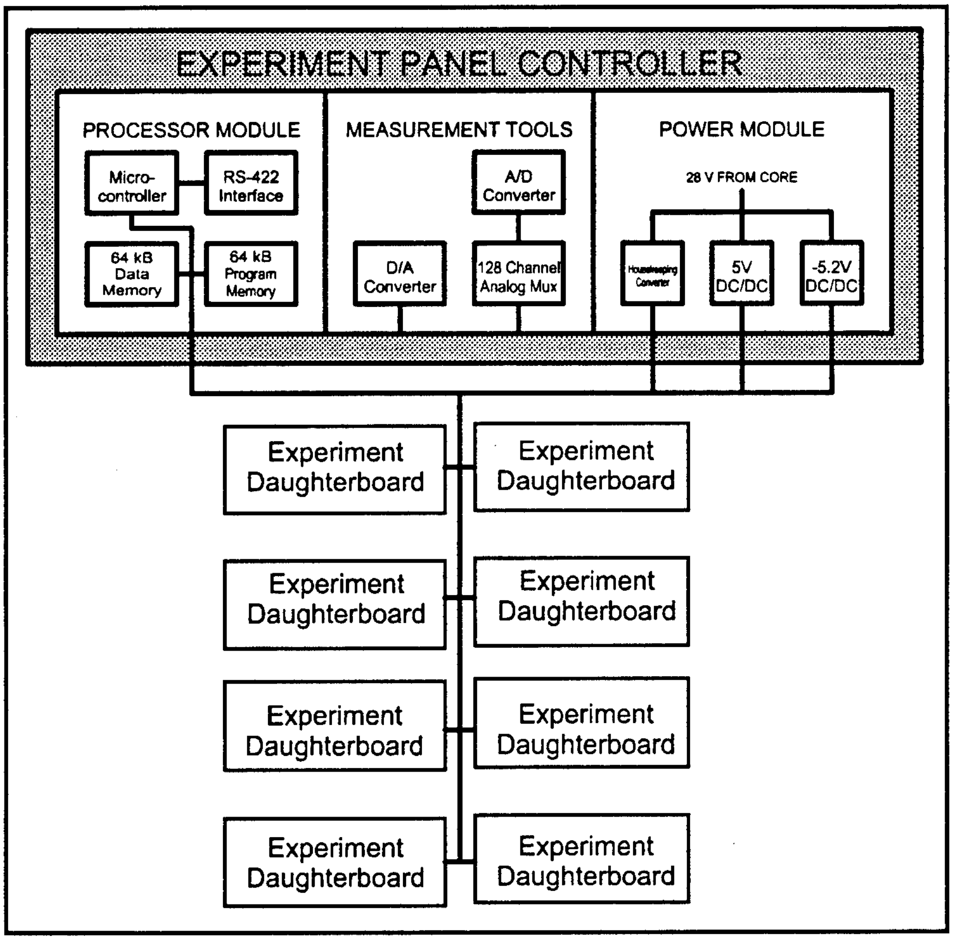

Figure 2: Experimental Panel Controller

Connection from the EPC to the daughterboard experiment is made via a 96-pin connector (part # ELCO 10-8477-096-002-904). The pin assignments are tabulated on the next page in Table 1.

Pin	Row A	Row B	Row C
1	ADDR0	ADDR7	DATA0
2	ADDR1	ADDR8	DATA1
3	ADDR2	ADDR9	DATA2
4	ADDR3	ADDR10	DATA3
5	ADDR4	RD*	DATA4
6	ADDR5	WR*	DATA5
7	ADDR6	INT*	DATA6
8	BD_SEL*	INT_RESET*	DATA7
9	unassigned	RESET*	unassigned
10	GND	GND	GND
11	GND	GND	GND
12	+5V	+5V	+5V
13	+5V	+5V	+5V
14	+5V	+5V	+5V
15	GND	GND	GND
16	GND	GND	GND
17	-5.2 V	-5.2 V	-5.2 V
18	-5.2 V	-5.2 V	-5.2 V
19	-5.2 V	-5.2 V	-5.2 V
20	GND	GND	GND
21	GND	GND	GND
22	+15 V	+15 V	+15 V
23	-15 V	-15 V	-15 V
24	ANA_RTN	ANA_RTN	ANA_RTN
25	ANA_RTN	ANA_RTN	D/A_REF
26	ANALOG1	ANA_RTN_S	D/A_V
27	ANALOG2	ANALOG7	ANALOG12
28	ANALOG3	ANALOG8	ANALOG13
29	ANALOG4	ANALOG9	ANALOG14
30	ANALOG5	ANALOG10	Dosim_G
31	ANALOG6	ANALOG11	Dosim_S
32	Temp_High	Temp_rtn	Dosim_D

Table 1: ELCO Connector Pin Assignments

The panel controller provides both electric power and communication to the daughterboard via the ELCO connector. Power supplies of interest include V_{CC} (+5 V), V_{EE} (-5.2 V), and GND. Communication of data from the daughterboard is available via an 11-bit address bus and an 8-bit data bus. The eleven bit address defines an address space of two kilobytes of shared memory space. These signals, as well as the memory read and write strobes from the EPC microcontroller, are sent via Harris HCS245MS bus transceivers. Figure 3 on the following page details this operation.

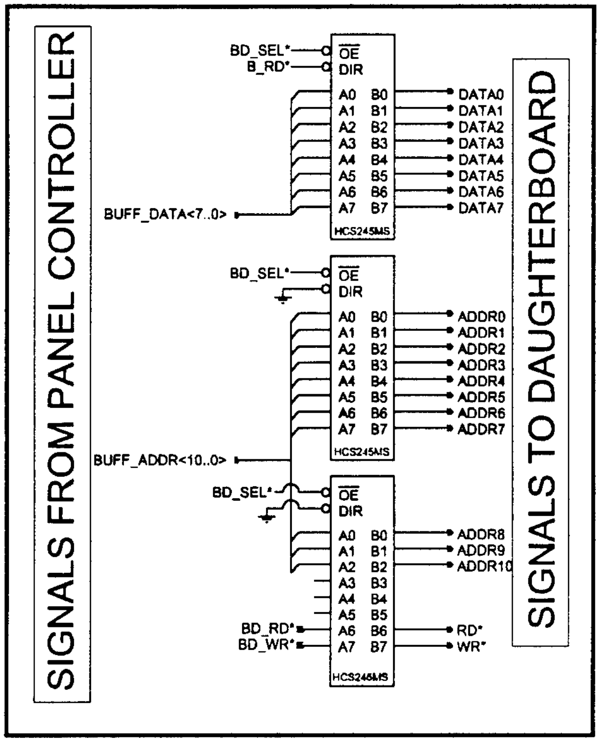

Figure 3: Daughterboard Communication Circuitry

These bus transceivers are mounted on the EPC motherboard. Output from the bus transceivers are connected to the 96-pin daughterboard connector. The DIR pins are tied to ground on the bottom two bus transceivers which sets the transmission direction from the panel controller side to the daughterboard side. The flow on the top transceiver is bi-directional. This DIR pin is tied to the EPC microcontroller read strobe to facilitate direction of data flow.

2. Communication Resources

Communication between the daughterboard and the EPC is accomplished via the address, data, read/write, and interrupt pins of the 96-pin connector. As indicated on Table 1, pins 5B, 6B, 7B, 8A, 8B, and 9B are assigned to RD*, WR*, INT*, BD_SEL*, INT_RESET*, and RESET*, respectively.

a. RD and WR**

These signals are individually driven low when the ECP microcontroller is reading from or writing to shared memory.

*b. INT**

The daughterboard can pull this line low to send an interrupt to the ECP microcontroller. The purpose of this is to tell the ECP that the daughterboard has data in shared memory to pass on. The daughterboard must not modify the data until the INT* line is reset by the ECP microcontroller.

*c. INT_RESET**

This line is driven low by the ECP microcontroller to reset a daughterboard INT* line. This is done when the ECP microcontroller has read the necessary data stored in shared memory. The ECP will keep this signal low until the daughterboard INT* line returns to a logical one level.

*d. BD_SEL**

This signal is driven low when the ECP microcontroller selects the daughterboard. From the time of the falling edge of this signal, the daughterboard has 657 nanoseconds [Ref. 2] until the EPC microcontroller takes control of the shared memory.

*e. RESET**

This signal is driven low by the ECP to reset all daughterboards.

3. Communication Interface

Data may be passed between the ECP and the daughterboard via two software protocols, Type 1 Interface and Type 2 Interface. Each interface is designed to be as modular as possible to facilitate the swapping of daughterboards if the need arose.

a. Type 1 Interface

Type 1 provides for a simple start/stop command structure. This protocol is envisioned for use on memory experiment daughterboards. It provides for recording the address range of a particular segment of a test and the test pattern used. It can report errors for specific addresses and error count for a time period. This method uses the INT* and INT_RESET* signal lines to control data flow.

b. Type II Interface

This interface is designed for experiments that require more complex commands and/or will generate complex or variable error messages. Since the daughterboard for this thesis will most likely use Type I Interface, no further comment shall be made.

IV. DAUGHTERBOARD COMPONENT SUMMARY

A. OVERVIEW

Circuit board design begins with a conceptual idea or a design proposal. An important aspect of turning a design proposal into a working design is finding a suitable place to start. For the MPTB daughterboard design, the place to start was with the microcontroller. There are many microcontrollers and microprocessors available to choose from. However, the requirement that the microcontroller needs to be radiation hardened greatly narrows the list of choices. With a microcontroller chosen, one may proceed with basic needs: memory, address decoding, non-volatile storage, etc. The next element to be considered is communication with the daughterboard panel controller. As the protocol for accomplishing this is usually dictated by the controlling device, it simply remains to implement the necessary signals. Once this is complete, one may wire up the memory chips to be tested to the microcontroller bus and control signals. From the aspect of a memory experiment, the daughterboard is essentially complete.

This chapter is dedicated to explaining the operation of the daughterboard. The first section will summarize the individual components on the board. Subsequent sections will explain the operation of various subsections of the design.

B. SUMMARY OF DAUGHTERBOARD COMPONENTS

From this point forward, the following convention shall be used. Pins with active-low signals will be designated with an asterisk. For example, a component with an active low chip-select pin, CS, shall be designated CS*. Datasheets for the following components are available in Appendix B.

1. UT69RH051 Microcontroller

The UT69RH051 is a radiation hardened CMOS microcontroller made by United Technologies Corporation (UTMC). The chip is based on the widely used Intel 8051 microcontroller and uses the same MCS51 assembly language. It has four 8-bit programmable I/O ports numbered Port 0 to Port 3. Port 0 and Port 2 are usually used as a 16-bit address bus, allowing it to address 65 kilobytes of memory. Port 0, which comprises the low byte of the address bus, is multiplexed with the 8-bit data bus. Read and Write strobes on Port 3 control external data reads and writes. Finally, the UT69RH051 has two pins on Port 3 for external interrupts.

2. UT22VP10

The UT22VP10 is a radiation hardened programmable array logic (PAL) made by UTMC. The TTL version was chosen because the it can source much more current to the outputs. This IC will be used to implement all random logic functions (AND, NAND, OR, NOR, NOT) in one IC. The UT22VP10 features up to eleven inputs and 10 outputs.

3. HS138MS

The HS138MS is a radiation-hardened 3-to-8 CMOS decoder made by the Harris Corporation. The purpose of this chip is to provide address decoding. The chip has three inputs (A0..2) and eight active-low outputs (Y7..0*). Chip select is accomplished via three enable inputs (E1*, E2*, E3), allowing up to three separate signals to control the device. All outputs have logical ones written to them when any one of the enables is not set This IC will be used for address decoding for the various memories on the daughterboard.

4. HCST541MS

The HCST541MS is a radiation-hardened 8-bit tri-state buffer. This IC is used to isolate components on the data bus when those components are not selected. The '541 has an 8-bit input (A7..0), 8-bit output (Y7..0), and two output enable pins (OE2*,OE1*). The separate output enable pins allow for added flexibility for output control.

5. HCS573MS

The HS573MS is a radiation-hardened 8-bit CMOS latch made by Harris. The purpose of this chip is to latch the lower byte of the address of the microcontroller. Recalling that the lower address byte of the microcontroller is multiplexed with the data outputs, the latch grabs the address byte to prevent address timing difficulties that may be encountered when a microcontroller addresses different types of memories with their own unique timing characteristics. The '573 has an 8-bit input (D7..0) and an 8-bit tri-state output (Q7..0). Chip operation is controlled by an active-low output enable (OE*) and an active-low latch enable (LE*). The latch is logically transparent when latch enable is high. Inputs are latched on a high-low latch enable transition. The '573 is functionally similar to the '373 latch commonly found on TTL/CMOS ICs. However, the '573 features a "broadside" pinout; that is, all inputs on one side and outputs on the other.

6. HS-6664RH

The HCS6664RH is a radiation-hardened 8k x 8 CMOS PROM made by Harris. The purpose of using this chip is to provide non-volatile memory storage for the daughterboard. The '6664 features a 13-bit latched address input (A12..0) and 8-bit tri-state data outputs (DQ7..0). The chip may be programmed by setting program select (P*) low. Two other inputs, chip select (E*) and output select (G*), control overall chip functions and output functions respectively.

7. HS-65647RH

The HS-656457RH is a radiation-hardened 8k x 8 CMOS SRAM made by Harris. The purpose of the '65647 is to provide memory space for the microcontroller to do calculations. The chip features a 13-bit address input (A12..0) and 8-bit tri-state data output (DQ7..0). Control signals consist of two chip select pins (E1*, E2), one output enable (G*), and one write enable (W*).

8. HS-82C85RH

The HS-82C85RH is a radiation hardened CMOS clock generator made by Harris. The purpose of the chip is to input an oscillating waveform and output a consistent, square-wave, clock signal. The chip has two crystal inputs (X1, X2). Three sets of control pins, a speed operation pin (FST/SLO), crystal/oscillator select pin (F/C), and three start/stop pins (S2..0) are used to control chip operation. Clock outputs are available in either a one-to-one ratio with the input (OSC) or a divide-by-three ratio with the input (CLK50).

9. 100328

The 100328 is an octal bi-directional ECL/TTL logic converter. A radiation hardened version is available from National Semiconductor. This IC is used to convert logic signals to and from the ECL memory chip to be tested on the daughterboard. Inputs/outputs (I/O) consist of eight TTL I/O pins (T7..0) and eight ECL I/O pins (E7..0). The logic level on the direction control pin (DIR) controls if the chip is in ECL-to-TTL or TTL-to-ECL mode. In either mode, outputs may be latched. The latch enable pin (LE) implements this function. Finally, a chip select pin (OE) enables the I/O pins. When not enabled, the ECL pins are cut-off and the TTL pins are tri-stated.

10. F10422

The F10422 is a 256 x 4 ECL SRAM made by National Semiconductor. This is one of four ICs to serve as experiment chips on the daughterboard. This chip has eight address inputs

(A7..0), four data inputs (D3..0), and four data outputs (O3..0). Output from individual data pins may be individually selected via four-bit select (BS3..0). A write enable (WE*) determines if data inputs or outputs are active.

11. VS12G422T

The VS12G422T is a 256 x 4 GaAs SRAM made by Vitesse. This is another of the four components to be tested for the daughterboard experiment. This chip has eight address inputs (A7..0), four data inputs (D3..0), and four data outputs (O3..0). A write enable (WE*) and an output enable (OE*) determines if the data inputs or data outputs pins are active. Chip select is accomplished via two pins (CS1*, CS2).

12. IDT6168

The IDT6168 is a 4k x 4 CMOS SRAM made by Integrated Device Technology, Inc. This chip is another IC to be tested for the daughterboard experiment. The chip has twelve address inputs (A11..0) and four data pins (I/O3..0). Output is entirely controlled by the logic level on the write enable pin (WE*). Chip select is accomplished via a single pin (CS*).

13. Experimental GaAs IC

This chip is an experimental gallium-arsenide IC being designed at the Naval Postgraduate School. The IC is a semi-autonomous test package. The chip writes test patterns to its own flip-flops, and detects and counts SEUs. Input is needed from an outside controller to select one of eight clock speeds, begin execution, and read output results. Three clock select pins (SEL2..0) determine clock speed. A one-to-zero transition on the reset pin (RESET) zeros the two SEU counters and begins execution. A one-to-zero transition on two output control pins (READ_SR, READ_LFSR) latches the current SEU count in the respective counters into two 8-bit output registers (SR7..0, LFSR7..0). The chip also produces two counter overflow signals (SR_OVERFLOW, LFSR_OVERFLOW) and one signal indicating operation has terminated (SEU_ON_RESET).

14. ELCO 10-8477-096-002-904

This connector is specified in the MPTB Interface Control Document as the connector for daughterboards.

15. Capacitors

a. Phillips Surface Mount

These capacitors are connected on all components between power and ground to filter off any AC current noise present from the switching of the component logic.

b. Panasonic NHE

This capacitor is used to filter any noise from the -2V power supply to the Experimental GaAs IC.

16. Resistors

a. Phillips Surface Mount

These surface mount resistors are used as pull-up resistors for various component which need pins tied to logical one.

b. Ohmite Vitreous Enamel Conformal

These resistors are utilized in lieu of the surface mount resistors when the amount of power dissipated is expected to be more than the surface mount resistors are designed to handle.

17. Crystal Oscillator

This is a quartz crystal made by Raltron. It provides an oscillator input to the Harris clock generator. A 36 MHz crystal is planned for the daughterboard. This is achieved by using the 3rd overtone of a 12 MHz fundamental frequency.

18. Zener Diode

This part is made by the Motorola Corporation. This element is used to regulate a -2 volt power supply for the experimental GaAs chip. Zener diodes maintain a specific voltage drop for varying currents. Thus, as the amount of current drawn by the GaAs IC varies, the diode will compensate for this and continue to supply -2 V.

C. COMPONENT ELECTRICAL REQUIREMENTS

The majority of the logic components of this design use +5V and Ground as a logical one and zero, respectively. Those parts that do not use these voltages have logic converters to translate their respective logic levels. However, components which use the same voltage levels cannot be automatically connected together and expected to function correctly. For component pins which drive signals to multiple ICs, such as data and address lines, a critical issue is whether those pins

can source or sink enough current. A manufactures datasheet usually provides two parameters, I_{OH} and I_{OL}, to determine how much current output pins can handle. I_{OH} is defined as the maximum current that the output can source when driving a logical one and still maintain the required minimum voltage level for a logical one, V_{OH}. I_{OL} is defined as the maximum current that the output can sink when driving a logical zero signal and still maintain an output voltage no greater than the maximum voltage for a logical zero, V_{OL}. The amount of current required for an output to source or sink is determined by Equation 4.1.

$$I_{SOURCE} = \sum I_{IH} + \sum I_{LEAK} \qquad \text{Equation 4.1}$$

I_{IH} is the amount of current an input draws when driven high. I_{LEAK} or "leakage" current is the amount of current a connected but not enabled input pin draws. The amount of current for an output pin to sink when driving a signal low is defined by Equation 4.2.

$$I_{SINK} = \sum I_{IL} + \sum I_{LEAK} \qquad \text{Equation 4.2}$$

I_{IL} is the amount of current drawn from an input pin when being driven low. I_{LEAK} in this case is the amount of current a connected but not enabled input pin sources.

A summary of input and output currents for the components to be used in the design are tabulated in Table 2:

Component	I_{OH} **(mA)**	I_{OL} **(mA)**	I_{IH} **(μA)**	I_{IL} **(μA)**	I_{LEAK} **(μA)**
'8051 Port 0	7.0	7.0	10	50	10
'8051 Port 1,2,3	0.06	3.5	10	10	10
UT22VP10	12.0	12.0	10	10	10
HS-6664RH	2.0	4.8	1	1	10
HS-65647RH	5.0	8.0	1	1	60
HS-82C85RH	2.5	5.0	1	1	5
HCS138MS	6.0	6.0	5	5	5
HCS573MS	6.0	6.0	5	5	5
HCTS541MS	6.0	6.0	5	5	5
VS12G422T	5.2	8.0	100	100	1000
IDT6168	8.0	4.0	10	10	10
F10422	n/a	n/a	220	50	n/a
100328 (TTL)	1.0	24.0	70	1000	70
100328 (ECL)	n/a	n/a	500	0.5	n/a

Table 2: Summary Of Component Pin Currents

An output pin usually cannot source enough power only when it is hooked up to multiple inputs. The only component on the design where this condition is present is the microcontroller. Port 0 of the '8051 is hooked up to the most components. However, referencing Table 2, these pins can source 7.0 mA current. With typical input loads of a few micro-amperes, no problem exists here. However, Ports 1, 2 and 3 can only source 60 μA to hold attached signals high. **This is a problem for only the write strobe on Port 3**. This signal is routed to two HS-65647 RAMs, the IDT6168, the VS12G422T, and one of the 100328s. Referencing Table 2, the input leakage currents to all the aforementioned chips totals 182 μA. Thus, the write strobe does not source enough current to maintain a logical one. Without correction, WR* is virtually tied low.

The solution is to tie this line high via a pull-up resistor. However, the resistor must be chosen such that it sources enough current to keep the line high when not active. It also must pull the line low when WR* is active. Equation 4.3 [Ref. 5, p.693] is used to calculate the maximum resistor value.

$$R_{MAX} = \frac{V_{DD} - V_{OH}}{m \times I_{IH} + \sum I_{LEAK}} \qquad \text{Equation 4.3}$$

Using values from Table 2, $V_{DD} = 5V$, and $V_{OH} = 3.2V$ (a conservative value),

$$R_{MAX} = \frac{5 - 3.2}{(100 + 1 + 1 + 10 + 70)} \approx 10{,}000\ \Omega$$

To calculate the minimum resistor value, Equation 4.4 is utilized.

$$R_{MIN} = \frac{V_{DD} - V_{OL}}{I_{OL} - \sum I_{L}} \qquad \text{Equation 4.4}$$

Using values from Table 2, $V_{DD} = 5$ and $V_{OL} = 0.4V$,

$$R_{MIN} = \frac{5 - 0.4}{3.5 - (1000 + 100 + 10 + 1 + 1)} \approx 2{,}000\Omega$$

Therefore, any value between 2-10 kW will allow the strobe to work correctly. Calculating the median voltage, the WR* signal is tied high via a 6 kΩ resistor.

D. TIMING ANALYSIS

Whenever memories and a microprocessor are tied together, the RAM speed must checked. One must analyze the timing diagrams of the components to ensure minimum and maximum setup, hold, and valid times are not compromised. Figure 4 below depicts the '8051 read cycle. The daughterboard will be using a 12 MHz clock. Therefore, each clock period, T_{CLK}, is 83 nanoseconds. Using this time to reference the UT69RH051 datasheet, two representative times are calculated for the microcontrollers memory access time parameters. The first, t_{LLDV} , is the time from when ALE goes low to the time valid data is present on the data bus. With an 83 ns period, t_{LLDV} = 514 ns. When ALE goes low on the daughterboard, the HCS138MS decoder chip is enabled. The maximum propagation time from enable to output for the decoder is 34 ns. This time must be subtracted from t_{LLDV} . The result, 480 ns, is the maximum time a memory chip has from enable to data-valid.

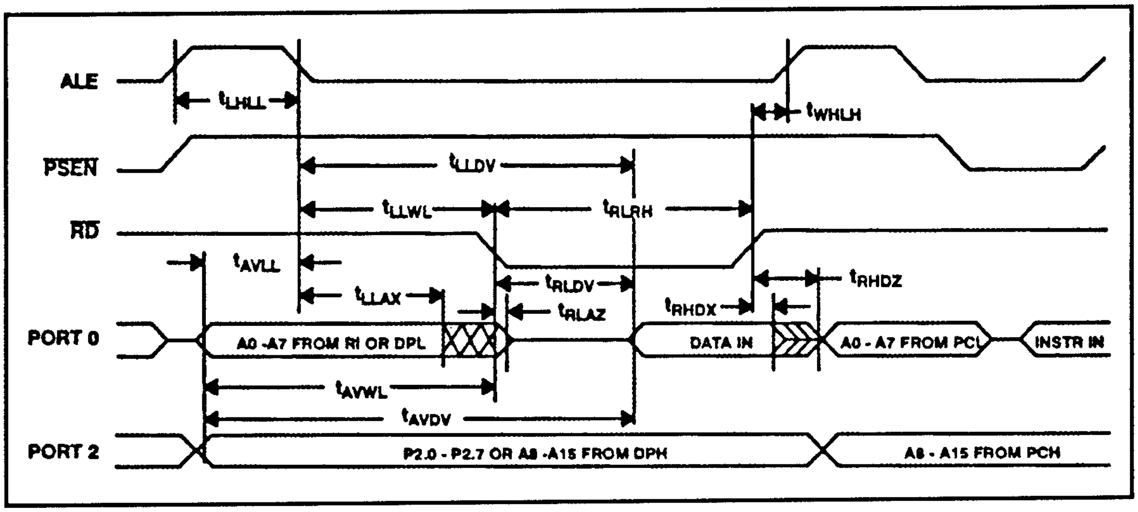

Figure 4: Microcontroller External Memory Read Cycle

Another critical access time is t_{RLDV}. This is the time from the read strobe goes active to the time valid data is present on the bus. This time at 12 MHz is 250 ns. The read strobe passes through the UT22VP10 PAL. This incurs a propagation delay of 25 ns. Thus, the access time is 225 ns. Table 3 below compares these times with the corresponding access times for all memories. As one can see, even the slowest SRAM can meet these maximum time by a wide margin.

Component	t_{LLDV}	t_{RLDV}
UT69RH051	480	225
HS-6664RH	60	20
HS-65647RH	50	15
F10422	10	n/a
VS12G422T	4	4
IDT6168	70	n/a

Table 3: Summary of Memory Access Time

The overall conclusion to be drawn from this is that all memories utilized in the daughterboard are significantly faster then they need be. However, one must bear in mind that the daughterboard is designed for testing radiation hardness, not speed.

V. DAUGHTERBOARD OPERATION

A. MICROCONTROLLER CORE SECTION

The microcontroller is the core of the entire daughterboard. This section consists of one UT69RH051 microcontroller, one HCS573MS latch, one HCS138MS decoder, two HS-6664RH PROMs, and two HS-65647RH SRAMs. Figure 5 on the next page depicts this section of the daughterboard.

1. Latch Connection

The first component connected is the HCS573MS ('573). The inputs of this device are connected to Port 0 of the microcontroller, LE* is connected to ALE*. When ALE* goes low, the lower byte the microcontrollers address is latched. Therefore, from this point forward, reference to the address bus shall include the upper byte coming from the microcontroller and the lower byte coming from the latch. Reference to the data bus shall pertain to the Port 0 pins of the microcontroller.

2. Decoder Connection

The next component to connect to the microcontroller is the HCS138MS ('138). Connecting address pins A15..12 to the A2..0 input pins of the '138, the 65k address space of the '8051 is divided into eight 8k segments. The outputs of the decoder, Y7..0, are used as enable signals for each segment. ALE* from the '8051 is wired to '138 enable E1* to synchronize the address decoding with the latch of the lower address byte of the '8051. Not doing this will cause components with latched address inputs to incorrectly decode the lower address byte. The other two enable inputs for the '138, E2* and E3, are tied low and high, respectively.

3. Combining PSEN* and RD*

The '8051 actually has the ability to address two separate 65k blocks of memory. Two read strobes, Program Store Enable (PSEN*) and External Data Read (RD*), exist on the microcontroller, The MCS51 assembly language has separate move instructions to choose between the two address spaces. In order to simplify programming, a common practice is to combine address spaces by wiring the two read strobes into an AND gate. Both strobes are active-low. Thus, when either is active, an active-low signal will appear at the output of the AND gate. From this point forward, this output will be referred to as "the" read strobe or "RD*" signal.

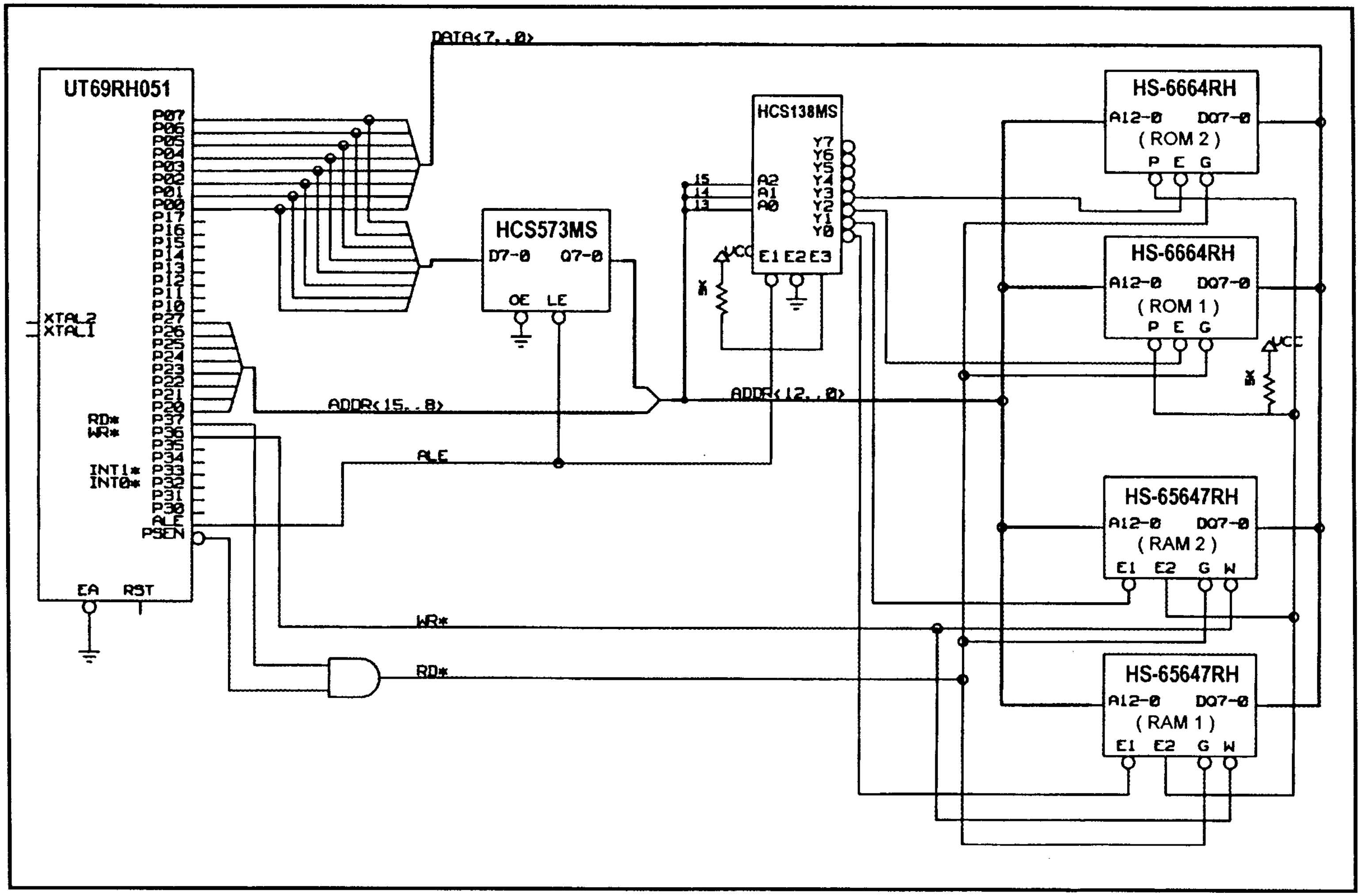

Figure 5: Microcontroller Core Section

4. SRAM Connection

It was decided that the amount of SRAM needed for the daughterboard was 16k. This was a compromise between using 8k, which had the possibility of being too small, and 32k, which took up half the address space of the '8051. Therefore, two HS-65647RH ('65647) are used. Wiring to the '65647s is straight-forward. Address pins A12..0 are connected to the address bus, data pins DQ7..0 are connected to the data bus. The board read and write strobes are wired to the output enable pin (G*) and the write enable pin (W*). Recalling the MPTB ICD specifies a shared memory space of 2 kilobytes, this necessitates that at least one of the '65647 chips must have the first 8k of address space. Therefore, the Y0* signal from the '138 decoder is connected to the chip-select pin, E1*, of the first '65647 (designated RAM1 on Figure 5). Y1* of the decoder is connected to E1* of the other '65647 (RAM2 on Figure 5). Together, the two SRAMs occupy a continuous memory space form 16k to 0. The final connections are to tie E2 on both SRAMs high since only one chip-select is necessary.

5. PROM Connection

It was decided that the amount of SRAM needed for the daughterboard was 6k. Two HS-6664RH ('6664) are used to implement this. Wiring to the '6664s is straight-forward. Address pins A12..0 are connected to the address bus and data pins DQ7..0 are connected to the data bus. The board read strobe is wired to the output enable pin (G*). The Y3* signal from the '138 decoder is connected to the chip-select pin, E*, of the first '6664 (designated ROM1 on Figure 5). Y4* of the decoder is connected to E2* of the other '6664 (ROM2 on Figure 5). Together, both ROM chips occupy a continuous memory space from 16-32k.

6. Clock Input

The CLOCK50 pin of the HS-82C85RH ('82C85) provides the '8051 with a 12MHz clock signal. This is connected to XTAL1 of the '8051, as depicted on Figure 6. The frequency source of the '82C85 is derived from a 36 MHz crystal oscillator connected to the X1 and X2 pins of the clock generator. Several pins on the '82C85 are tied either high or low to set the desired operation of the chip. The F/C pin is tied low to select crystal oscillator input. The FST/SLO pin is tied high so that the output on the OSC and CLOCK50 pins are 36 MHz and 12 MHz, respectively (selecting low has a divide by 768 effect). Finally, S2*, S1, and S0 are tied high, low and low respectively to disable the stop-clock function. Connection to the crystal is done via two

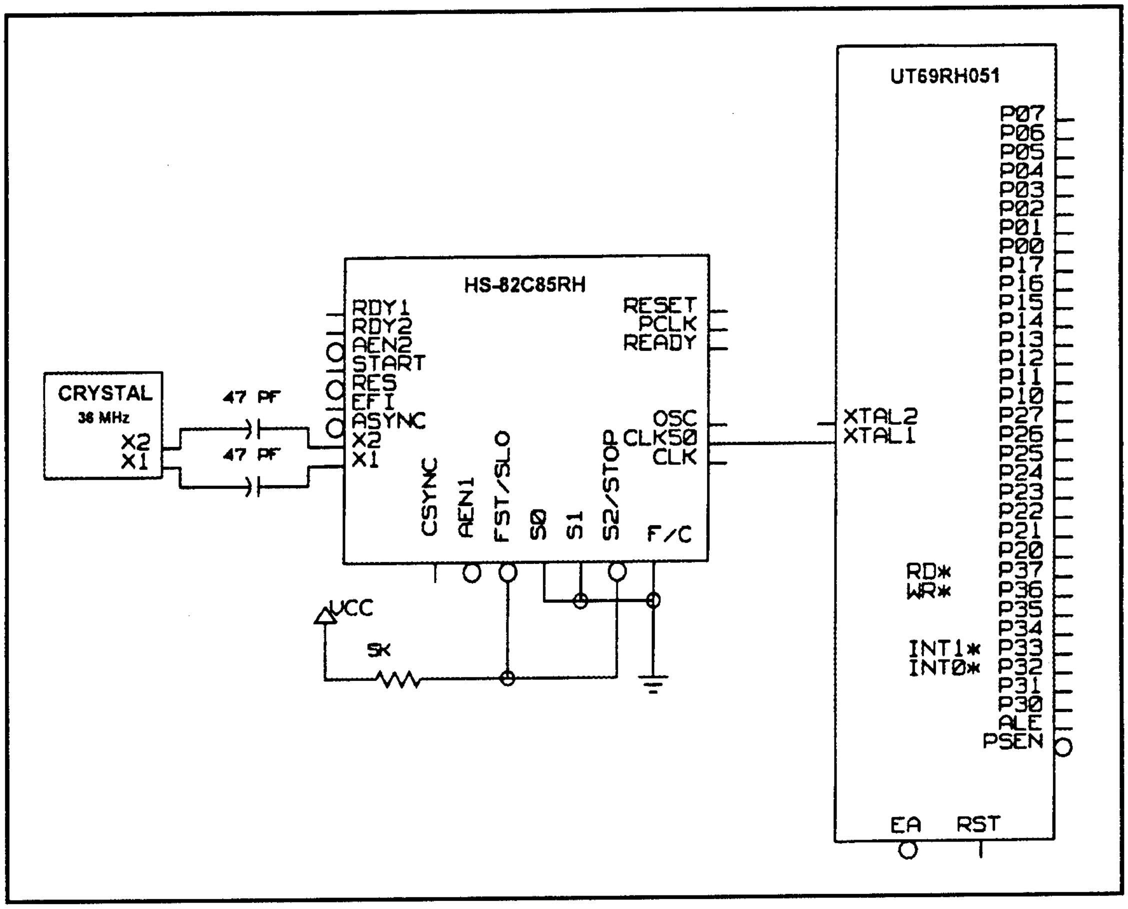

Figure 6: Daughterboard Clock Signal Source

47 pF capacitors in order to provide the most stable operation of the OSC output (which provides the clock to the experimental GaAs IC). This is accomplished by matching the load capacitance of the crystal to the combined capacitance of the capacitors. This relationship is defined in Equation 5.1 below.

$$C_{crystal} = \frac{C_1 \times C_2}{C_1 + C_2} \qquad \text{Equation 5.1}$$

The load capacitance of the crystal is 24 pF. Therefore, C1 =C2 = 48 pF. The closest capacitors available is 47 pF (+/- 5 %).

7. Miscellaneous Microcontroller Connections.

The '8051 has 256 words of internal memory. This unnecessarily complicates the memory address space and is not recommended to use. This memory is of little use because of its small size

and complicates microcontroller programming. Wiring EA* on the microcontroller to ground disables this memory.

B. SATELLITE INTERFACE SECTION

As previously stated, communication between the daughterboard and the EPC via a 96-pin connector. The communication signals between the two components was discussed in Chapter III. Actual connection is depicted in Figure 7. This interface has three basic operations. First, the EPC requests attention from the daughterboard via an interrupt. Second, the daughterboard may interrupt the EPC. Third, the daughterboard transfers information to the EPC.

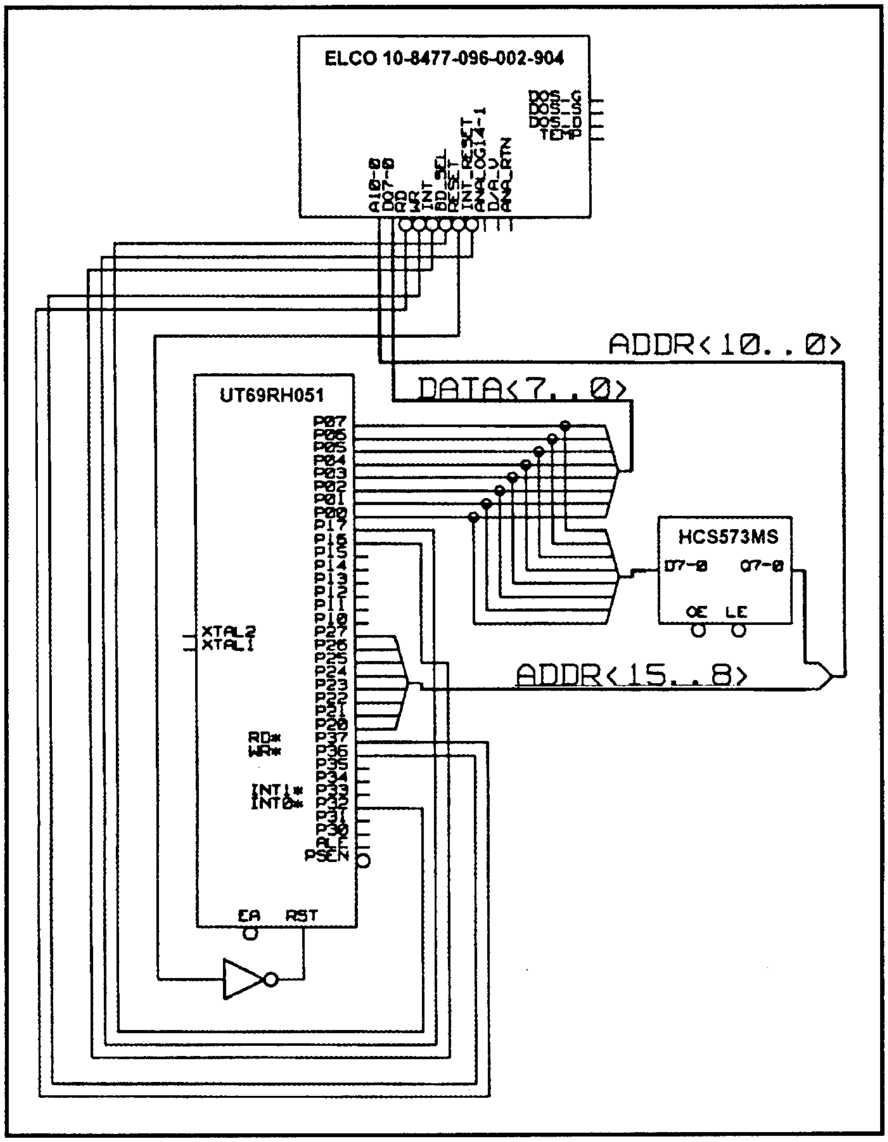

Figure 7: Interface To Satellite

1. Interrupt From EPC To Daughterboard

The BD_SEL* signal from EPC is connected to the INT0* pin of the '8051 microcontroller. When the EPC drives the BD_SEL* signal low, it activates Interrupt 0 on the daughterboard microcontroller. As previously stated, the daughterboard has 657 nanoseconds before the EPC microcontroller begins to access the shared memory in the Harris SRAM. When the EPC has finished its memory access, it negates the BD_DEL* signal, allowing the daughterboard microcontroller to resume processing.

2. Interrupt From Daughterboard To EPC

The daughterboard '8051 may send an interrupt to the EPC. The daughterboard must then wait for a response from the EPC. When the EPC responds, it will initiate a read from shared memory. Implementation of this handshaking protocol is implement by connecting the INT* and INT_RESET* from the EPC via the connector, to '8051 Port 1 pins 7 (P1.7) and 6 (P1.6), respectively. This implements a handshaking protocol between daughterboard and panel controller.

Any '8051 Port pin may be programmed, provided the pin is not being used to fulfill another task. Ports 0, 2, and 3 of the microcontroller are used for the address bus, data bus, read/write strobes, and interrupts. Until this point, the Port 1 pins are unused. Thus, a subroutine may be written to drive P1.7 low to send an interrupt to the EPC. The subroutine can then instruct the daughterboard '8051 to poll P1.6 for a response. When the EPC drives INT_RESET* low, the daughterboard would have the attention of the EPC, allowing data transfer to take place. Using the Port pins in this fashion works well in this case because the microcontroller initiates contact and knows it only has to poll for a response for a limited time. If contact was not initiated from the daughterboard, the microcontroller would be forced to continuously poll a Port pin(s). This would be taxing on the microcontrollers resources.

3. EPC Accessing Shared Memory

The EPC has access to the daughterboards lower 2 kilobytes of address space and the boards data bus. The read and write strobes from the connector are connected to the read/write signal lines of the daughterboard. Once communication is established between daughterboard and EPC, R/W cycles proceed uneventfully.

C. MEMORY TEST SECTION

This section contains the three memory chips of different logic families. ECL-TTL level converters are required for the ECL SRAM. Additional logic gates are required for address decoding. Figure 8 depicts the logical layout.

1. CMOS SRAM

Connection of the IDT6168 ('6168) is straight-forward. Its address pins (A11..0) are tapped into the lower 12 bits of the daughterboard address bus. The data pins (I/O3..0) are tapped into the lower four bits of the data bus. R/W cycles are controlled exclusively by the write-enable pin, WE*. If the chip is selected and WE* is not asserted, a read operation is completed. The chip-select pin CS* is connected to the Y4* output of the '138 decoder. This allocates the '6168

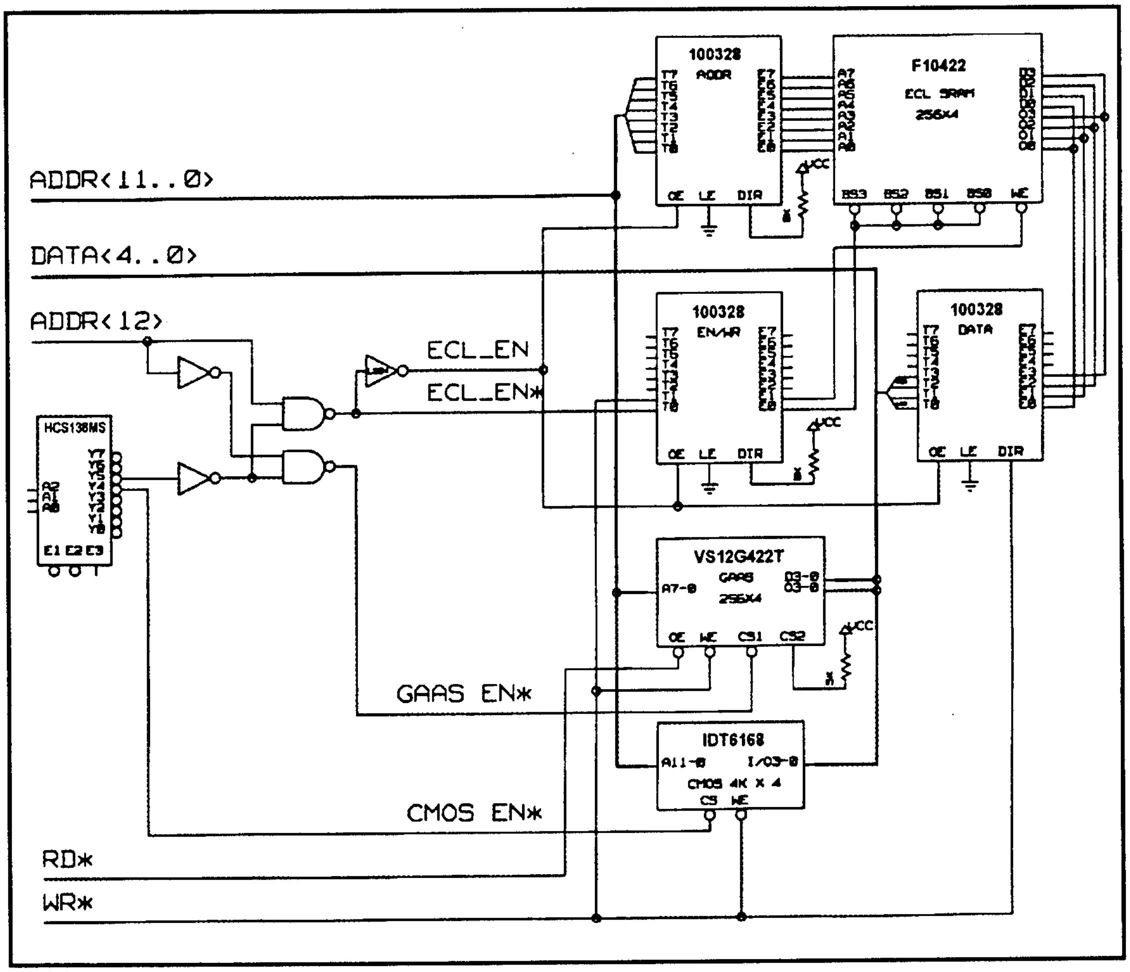

Figure 8: Test Memory ICs

address space 32k to 40k. However, the chip only utilizes the lower half of its allocated 8k address memory space. The upper 4k of the memory space is unused. This inefficient use of address space was chosen to minimize the number of gates required for address decoding.

2. GaAs SRAM

Connection of the VS12G422T ('422T) requires its address pins (A7..0) to be connected to the lower byte of the daughterboard address bus. The separate data input and data output pins are connected to their respective data bus lines. The microcontroller read and write strobes are connected to OE* and WE*, respectively. The '422T is allocated memory address space from 40k to 44k. Decoding of this address space is accomplished by routing theY5* output of the '138 decoder and the A12 address line into a 1-to-2 decoder. The 1-to-2 decoder is implemented in Figure 8 with two NAND gates and two inverters. This divides the 8k address space defined by the decoder into two 4k blocks. The '422T is allocated the lower half by connecting the CS1* pin of the '422T to the lower NAND gate of the 1-to-2 decoder. The '422T only uses 256 of the 4,000 locations it is allocated.

3. ECL RAM

Connection of the F10422 ('422E) is considerably more involved. ECL technology uses -5.2 volts and ground for logical zero and one, respectively. Thus, all signals to and from the ECL SRAM must pass through 100328 ECL-TTL logic converters. Three 100328s are required to implement translate all necessary signals to and from the ECL chip. The first converter is subtitled "ADDR" in Figure 8. The lower byte of the daughterboard address bus is routed to the TTL side. The signals come out the ECL side and into the address pins of the '422E. The 100328s are bi-directional. Since address information only propagate from the TTL side to the ECL side, the DIR pin of this converter is tied high so that signals only travel in the desired direction.

The lower four data bus lines of the daughterboard are connected to the TTL side of the 100328, labeled "DATA" in Figure 8. The signals route from the TTL side to the ECL side into the corresponding data-in pins (D3..0) and data-out pins (O3..0). Since the data lines need to be bi-directional, the DIR pin of this 100328 is connected to the read strobe of the daughterboard. On read operations, the read strobe is at logic level zero, allowing information on the 100328 to flow from the ECL to the TTL side. During memory write operations, the read strobe is at logic level one, which sets the converter to allow data to travel from the TTL side to the ECL side.

The third 100328, subtitled “RD/WR” on Figure 8, is utilized to pass the daughterboard read and write strobes to the ‘422E. These signals could not be sent through the “DATA” 100328 because when the direction of the converter is set in the ECL to TTL direction, the read and write strobes would be cut off. Therefore, the separate IC was required. The read strobe outputs the ECL side of the 100328 and connects to the four select lines, BS3..0 of the F10422. There is no need to individually access the data output lines, so all four are shorted together. The write strobe proceeds from the logic converter and connects to the write enable pin, WE*. The signal direction on this 100328 is exclusively from the TTL side to the ECL side, so the DIR pin is tied high.

Finally, the ECL SRAM is allocated address locations 44k to 48k. Address decoding is accomplished using the other output of the 1-to-2 decoder described in the GaAs SRAM section. This enable line is not connected to the ‘422E, but tied to the OE pins on all three 100328s. When the address decoders select the ECL SRAM, they enable the logic converters to allow transactions to the ECL chip to occur. When not selected, the TTL side of the three 100328s are in the high impedance state, effectively isolating the ‘422T.

D. EXPERIMENTAL GALLIUM-ARSENIDE IC

The operation of this chip has been described previously. However, considerable logic is required to implement its operation. Figure 9 logically depicts this part of the daughterboard. Operation of the circuit is describe in the following subsections.

1. Address Decoding

The Experimental GaAs chip (‘XGaAs) is allocated address space 48k to 56k. This address space is used to provide four enable lines for three HCST541MS (‘541) tri-state buffers and one HCS573MS (‘573) latch. Address lines A12 and A11 input to a two-to-four decoder which is created from four AND gates and two inverters. These outputs are each input into a NAND gate with the Y6* output of the ‘138 decoder. The ‘138 output acts a master enable signal. The net effect is that four active-low enable signals are created, INPUT_EN*, SEU_EN*, LFSR_EN*, and SR_EN*. Utilization of these signals is described shortly.

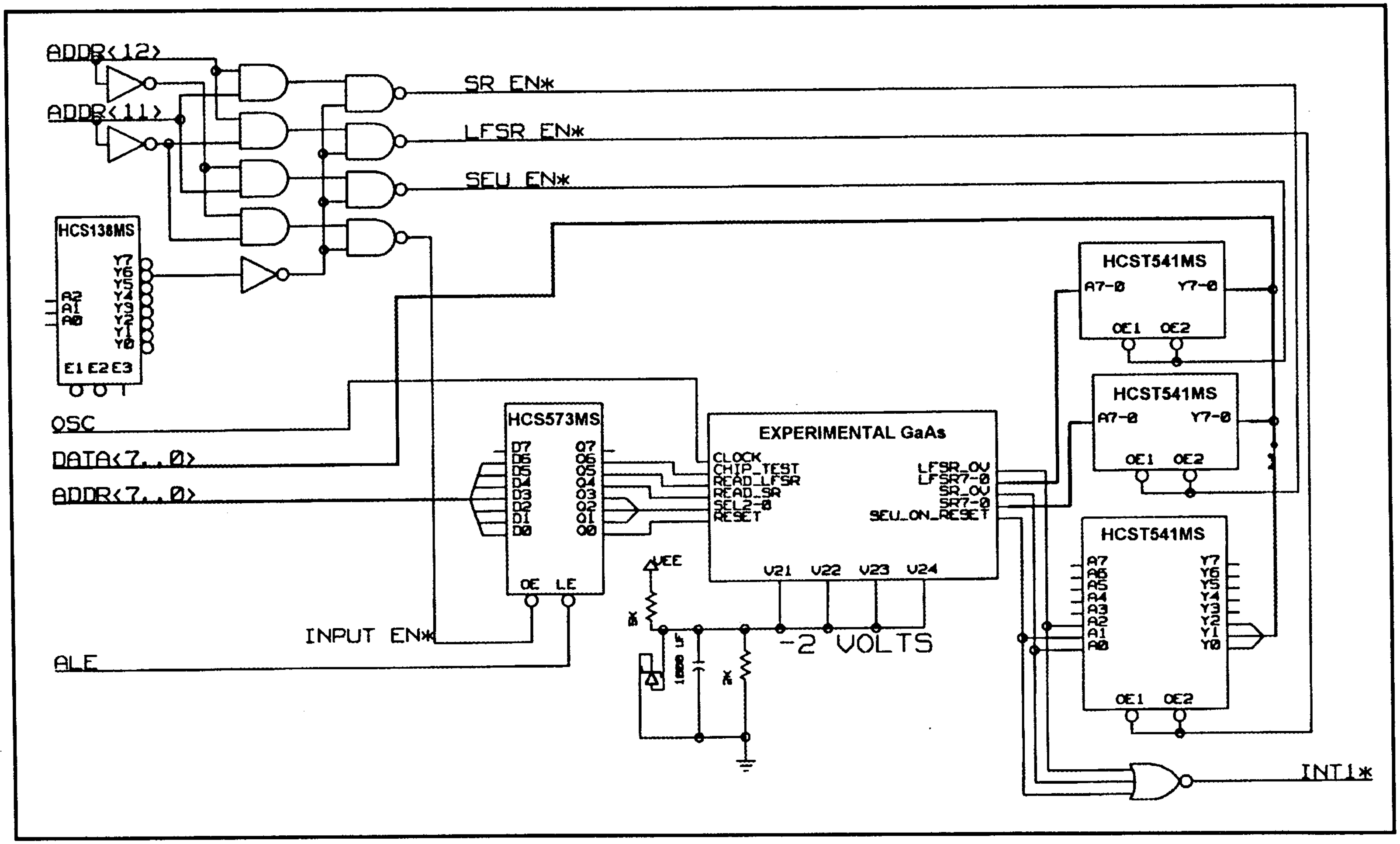

Figure 9: Experimental GaAs IC Implementation

2. Control Inputs

The ‘XGaAs has seven inputs to control chip operation. To manipulate these control lines, the outputs of a ‘573 latch is utilized. The inputs to the latch are connected to address lines A6..0. The INPUT_EN* is connected to the chip-select pin, OE* of the ‘573. The ‘8051 ALE* signal is attached to the LE*. Recall that when ALE* goes low, the inputs are latched on the output side of the ‘573. Therefore, when the latch is selected via address decoding of address lines A15..11, variations of A6..0 may be used to provide up to 2^7 separate input signals to the ‘XGaAs.

3. Reading Counter Outputs

Recall the ‘XGaAs has two counter outputs, LFSR7..0 and SR7..0. These outputs are not tri-stated. In order to connect them to the daughterboard data bus for reading, the ‘541 tri-state buffers must be utilized to isolate these signals when not selected for reading. The inputs of two of the buffers are connected to the two counter outputs. The LFSR_EN* enable signal is connected to the output select pins, OE1..0, of the ‘541 which is connected to the inputs LFSR7..0. The SR_EN* signal is connected the tri-state buffer that is connected SR7..0. Thus, the proper address decoding to activate either of the enable inputs will select the corresponding counter to be read.

4. Responding To Interrupts

Recall that the ‘XGaAs has three active-high interrupt signals. Unfortunately, the ‘8051 only has one remaining external interrupt. In order to accommodate this problem, the three interrupt signals form the ‘XGaAs are routed to the inputs of a three input NOR gate. The output of this gate is connected to the remaining external interrupt pin on the microcontroller, INT1*. Each of the three signals are also routed on the low three bits of the data bus via another ‘541 buffer. The SEU_EN* signal is connected to the OE1..0* pins of the tri-state buffer. Therefore, if one or more of the three interrupt signals goes active, this will produce a logic zero on the NOR gate, subsequently sending an interrupt to the microcontroller. An interrupt handling subroutine may be written to perform a read to the ‘541 buffer if an interrupt is detected. The read bits could then be tested to determine which of the three interrupt conditions was activated. The interrupt handling subroutine could then take appropriate action.

5. Power Supply

The ‘XGaAs presents a unique problem in that it requires a negative two volt power supply. This is the only instance on the entire daughterboard where the required power supply is

not provided by the EPC. The two resistors, one capacitor, and one zener diode depicted in Figure 9 forms a voltage regulator circuit that produces the required -2 volts. The circuit uses the -5.2 available voltage supply. A 5 kΩ resistor and a 2 V zener diode are connected in series to ground. The diode serves to stabilize the voltage if fluctuations in the current drawn occur. The voltage between the resistor and the diode is at the required -2 V. A 1000μF capacitor is connected in parallel to ground to filter off any AC noise. Finally, a 2 kΩ resistor is added to complete the circuit. The four pins depicted on the bottom of the 'XGaAs chip in Figure 9 are four pins that require the -2 V power supply. Thus, at the point shown in the diagram, a stable -2 V source is available for the 'XGaAs IC.

E. PROGRAMMABLE ARRAY LOGIC

The previous sections each had basic logic gates decoding address space, inverting signals, etc. These gates were shown in each section in order to make each section more understandable. The finished daughterboard design actually implements all of these gates in a single UT22VP10 PAL. Figure 10 on the next page shows the PAL with its input and outputs labeled with the assigned signals. The various logic gate structures utilized in the design are shown for reference.

F. COMPLETE DAUGHTERBOARD DESIGN

The complete logical design for the MPTB motherboard is a compilation of all the previous sections. Figure 11 on page 37 shows the entire design. Each of the previous sections previously discussed is incorporated. Within each design subsection, placement of components relative to one another is the same as in Figure 11. However, note that all logic gates have been remove and the PAL displayed in their place.

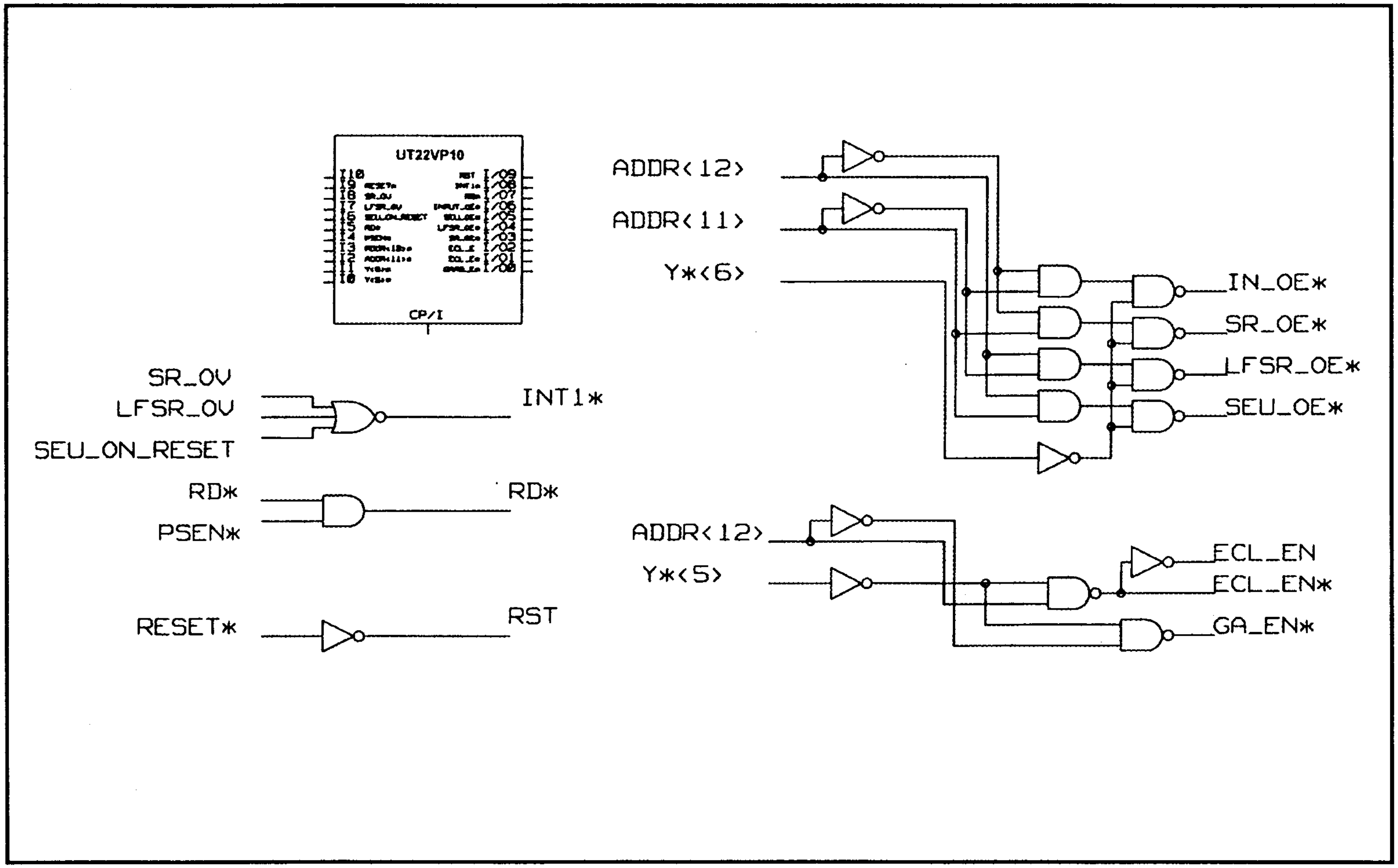

Figure 10: Summary Of PAL Logic

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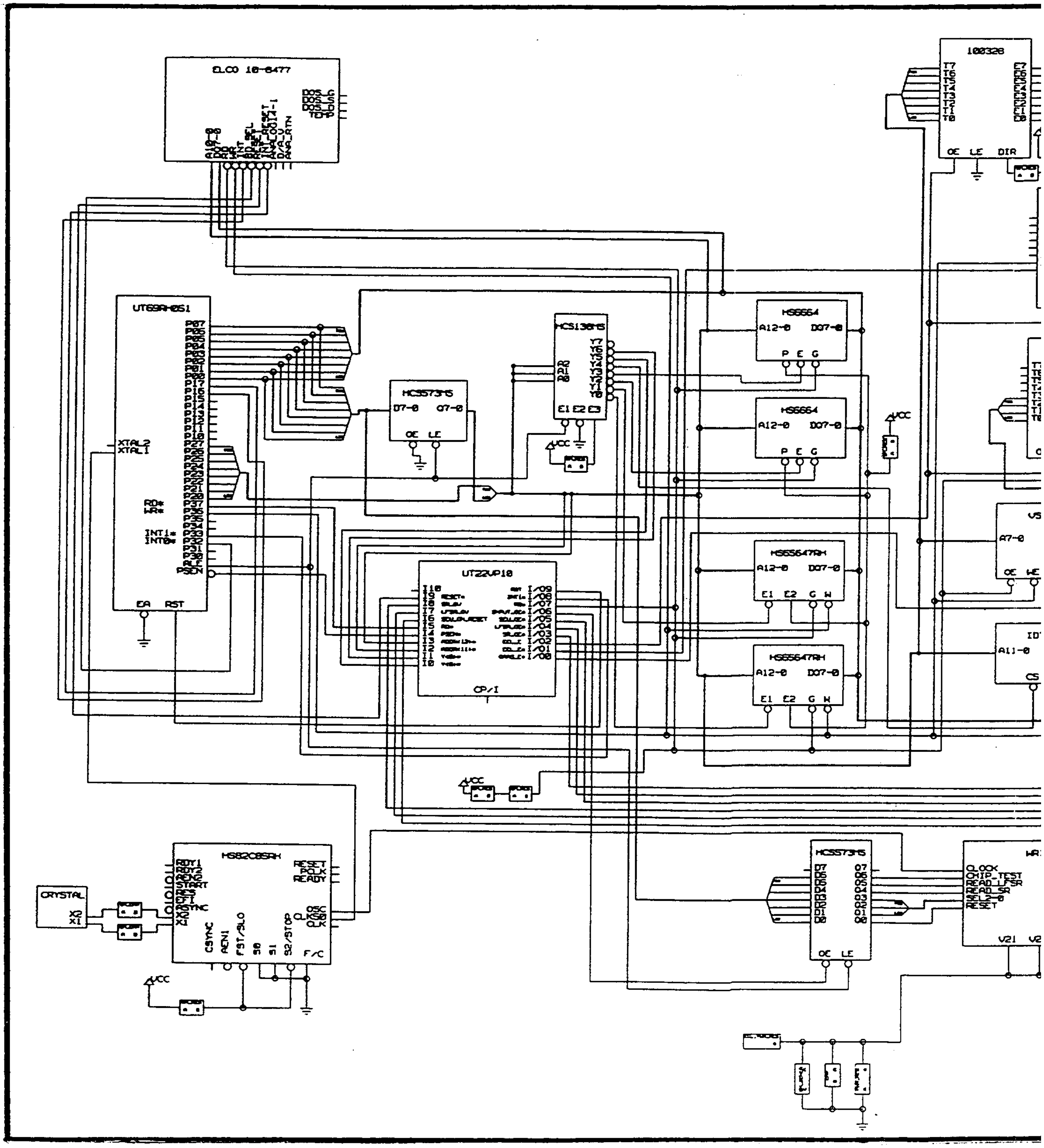

Figure 11: Complete Daughterboard Design

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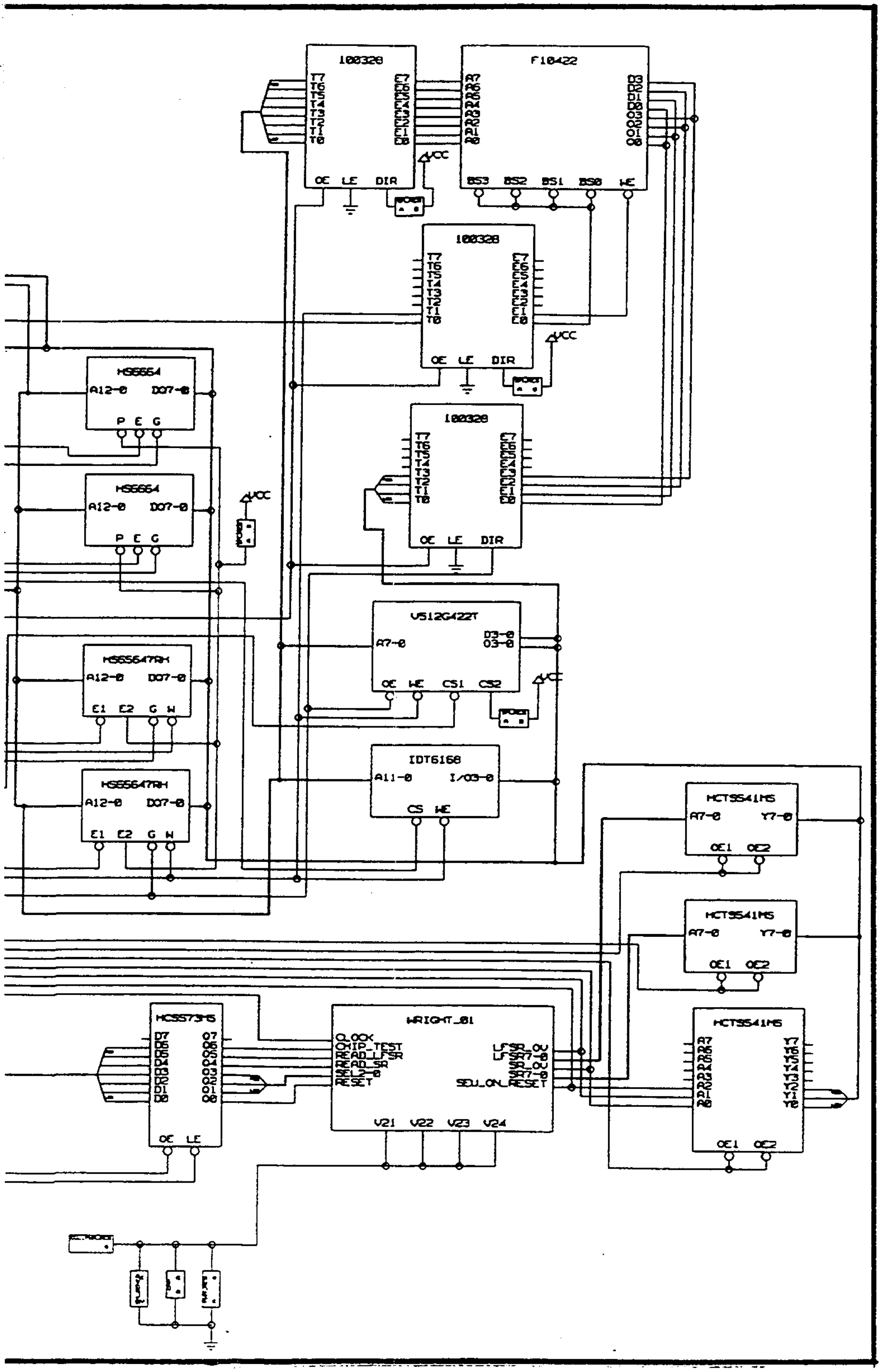


te Daughterboard Design

VI. CADENCE BOARD DESIGN TOOLS

A. OVERVIEW

The Cadence Board Design Tools are a subset of CAD tools of the greater Cadence CAD tool set. Design begins concurrently in Rapid Part and Concept. Rapid Part is a component library development tool, Concept is a schematic capture tool. Once complete, the information is compiled into a net-list for input into Allegro. Allegro is a CAD tool for designing a printed circuit board, including wiring and component layout. Output from Allegro may be sent to a printed circuit board company for board fabrication

The following sections contain a summary of the use of each CAD tool to give an idea of a beginning to end board design in Cadence. Also mentioned are some tips and tricks to help with the programs.

B. RAPID PART

The purpose of Rapid Part is to produce a symbol that reflects the correct pinout of a component one intends to use. If a component comes in several package types, Rapid Part can generate multiple versions of the same component, ie DIP, flatpack, quad-flatpack, etc. Another key piece of information inputted is the JEDEC type of each package. A JEDEC is the footprint a particular IC package makes on a printed circuit boards. It contains precise information on pin-hole spacing and pin-hole size for the actual design of the board. Appendix B of the Allegro Library Development manual contains a listing of standard JEDECs . If the correct footprint is not available in the Allegro library, the user has the ability to make their own.

C. CONCEPT

Once a library of parts has been created in Rapid Part, or at least enough components have been created to get started, Concept is used to logically wire the components together. Before using the program, it is strongly recommended that the Concept Stopwatch Design Tutorial be completed in order to become familiar with Concept. This tutorial is an efficient method to learn the program.

When initially setting up the program in GLOBAL SETUP, component libraries needed for the design must be entered. For basic logic design, the following libraries need to be included: LSTTL, ELEMENT, STANDARD, and any local libraries. LSTTL will give one a complete library of logic gates with standard symbol shapes. The ELEMENT library contains basic discrete

components such as resistors and capacitors. If a pin needs to be tied high or low, the ELEMENT library contains VCC and GND. The STANDARD library contains the full set of MERGES and TAPS. Any local libraries will contain parts created in Rapid Part.

An important issue not covered in the tutorial is the management of busses. It is recommended one thoroughly read the uses of TAPS and MERGES in the Concept Schematic User Guide. A tap is used to split off a subset of lines from a larger bus. When the TAP is used, signals split off bear the same signal name and properties. For instance, if one has an eight-bit bus called DATA<7..0>, using the command TAP 6..3 will tap into lines 6, 5, 4, 3. A wire connected to this tap will automatically inherit the signal name DATA<6..3>. MERGES can also be used to divide buses. However, since the number of total lines coming in one end of a merge must equal the number lines of exiting, one of the outputs from the merge must be left dangling with the appropriate unused signals assigned to it.

Concept deals with the connection of signal pins. A problem arises as power and ground pins are not usually shown. On a circuit board, it is a standard practice to wire a capacitor between the power and ground pins to filter off any AC noise generated from switching logic. But with no power and ground pins on the logic symbols, accomplishing this is confusing. The solution is to place a capacitor next to the logic component and connect the ends of the capacitor to VCC and GND symbols in the ELEMENT library as shown in Figure 12. This will allow connections

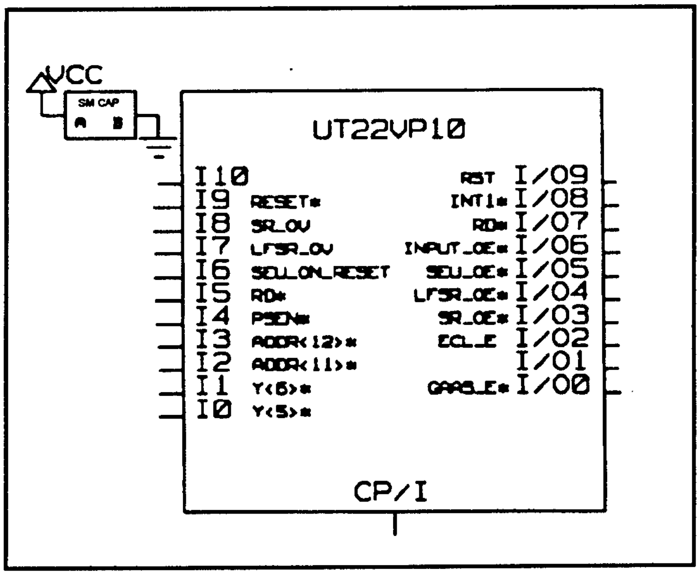


Figure 12: Placing Capacitors

between the capacitors to the power and ground pins on each component in Allegro. Not taking this step will cause Allegro to mark a design error.

D. VALID COMPILER AND PACKAGER XL

Once a logical design is complete, one needs to run the design through Valid Compiler and Valid Packager to format the design to import into Allegro. Valid Compiler produces a net-list. This is simply a file that lists every electrical connection between all components. Packager XL is a program that combines gates of the same type into one IC. For instance, when AND gates are placed on a design, they are placed individually. Most AND gate components usually incorporate several gates in one IC package. Thus, if a design has 32 OR gates, twenty-five inverters, and 37 AND gates, Packager XL will group the gates in "real-world" components which have 4, 6, 8, ... components per IC.

E. ALLEGRO

1. Library Development

More time is usually spent in Cadence creating and modifying libraries than anything else. Recall that in Rapid Part a JEDEC type or physical footprint was specified. At this point any JEDEC types not in the Allegro library must be created. JEDECs are defined by corresponding symbols in order to use them in Allegro. A symbol consists of two elements, padstacks, and drawings. For printed circuit boards, component pins are mounted in holes or on pads. A printed circuit board typically consists of 4 to 7 layers. A padstack simply defines how a hole or pad interacts with each individual layer. The "drawing" is simply a physical representation of the device. The drawing, with one or more padstacks, is combined to form a symbol.

2. Prepare Design

The first part of preparing a design for a printed circuit board is to define the boards outline. Once this is drawn, the cross section of the board is defined. For example, a four layer board would be defined such that wires could be routed on the top and bottom layer. The middle two layers are usually thin planes of copper connected to V_{CC} and GND. Once this is complete, CONSTRAINTS are defined. CONSTRAINTS are definitions of wire width, minimum spacing between components, spacing between wires and spacing between wires and component pins. The last steps are to add the Component and Route KEEPINS. KEEPINS are boundaries defined for the placement of components and wires. When components are mounted on a board, a minimum

distance from the board edge to place the components must be defined The same must be defined for wires. KEEPINS simply define these boundaries to keep components and wires from getting closer to the edge of the board than desired.

3. Placing Components

At this point, the design has the board defined. Components are ready to be placed. Placing components is application of common sense. The ultimate goal is to place the components to minimize the amount of wiring needed. For the daughterboard design, the following placement decisions were completed.

- The microcontroller was placed next to the designated address and data pins on the ELCO connector.
- The '573 latch and '138 decoder were placed next to the microcontroller since all memory transactions utilize these components.
- The two Harris SRAMs and PROMs were placed together due to similar pinouts allowed efficient busses to be wired.
- The test memories and the 'XGaAs IC were placed adjacent to one another.
- The 100328 logic converters were placed next to the ECL SRAM.
- Capacitors, resistors, and other discrete elements were placed next to the pins of components they were connected to.
- The 'XGaAs IC was placed near the edge of the board to aid in mounting.

Figure 13 on the next page shows the final placement of the daughterboard components.

4. Routing

Routing wires is the most dynamic and time consuming design process. The Automatic Router is recommended to begin routing with. The highest success rate occurs when the autorouter is started before a single wire is manually placed. The autorouter wires in a "Manhattan" style. For instance, if the printed circuit board has two board layers to make connections on, the router connects all the horizontal lines on one layer and the vertical wires on the other layer. Interactive routing method may be used to finish the routing, and/or clean up the design. Once the wires are complete, power and ground planes are defined in the internal layers of the board. A function called auto-voiding automatically creates holes in the planes for pins not directly connected to either plane. Auto-voiding will also connect V_{CC}, V_{EE}, and GND pins of each component to the

appropriate plane. Figure 14 on page 44 shows the routing on both sides of the circuit board. Figures 15 and 16 on pages 45 and 46 show routing on the top and bottom layers, respectively.

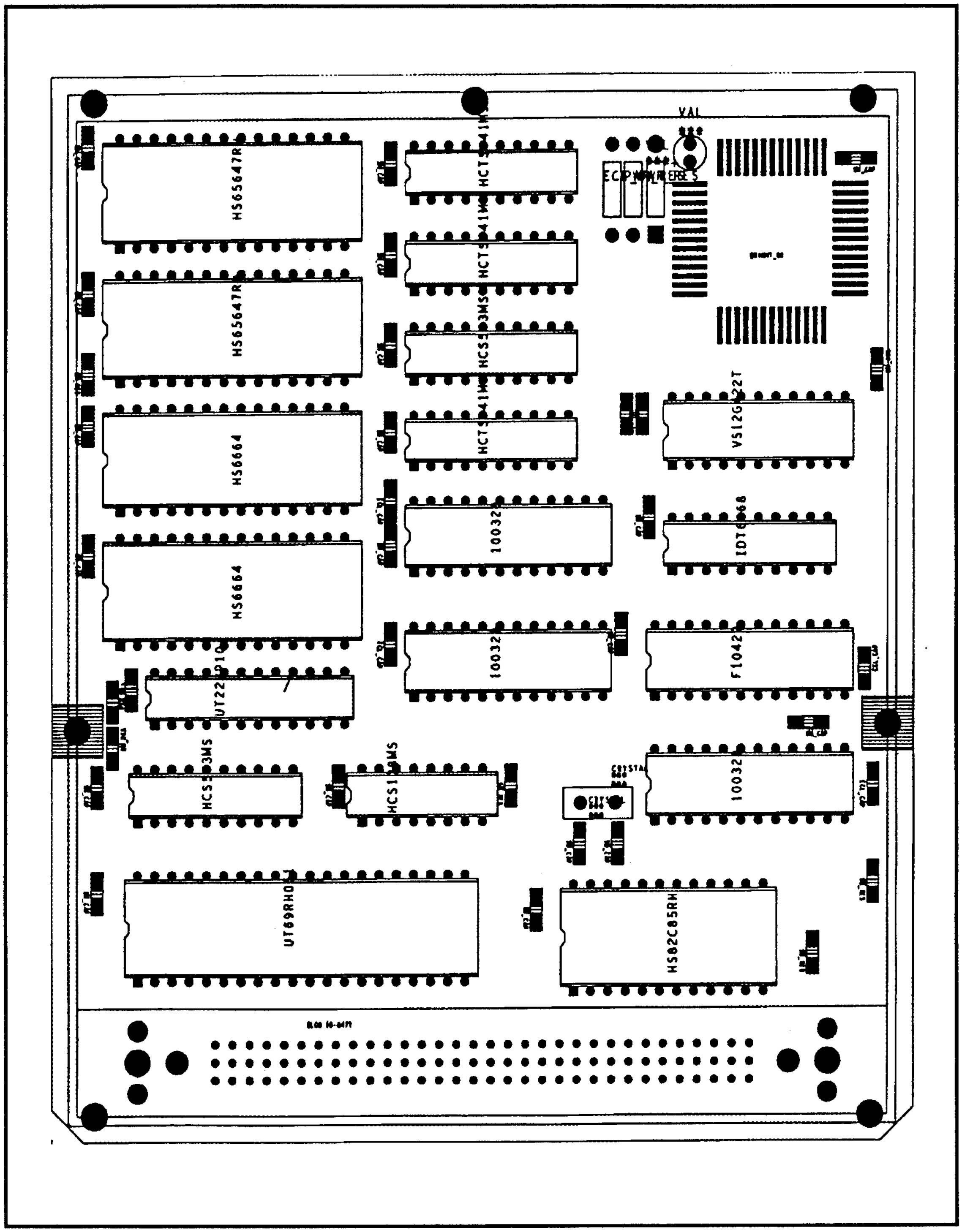


Figure 13: Daughterboard Component Placement

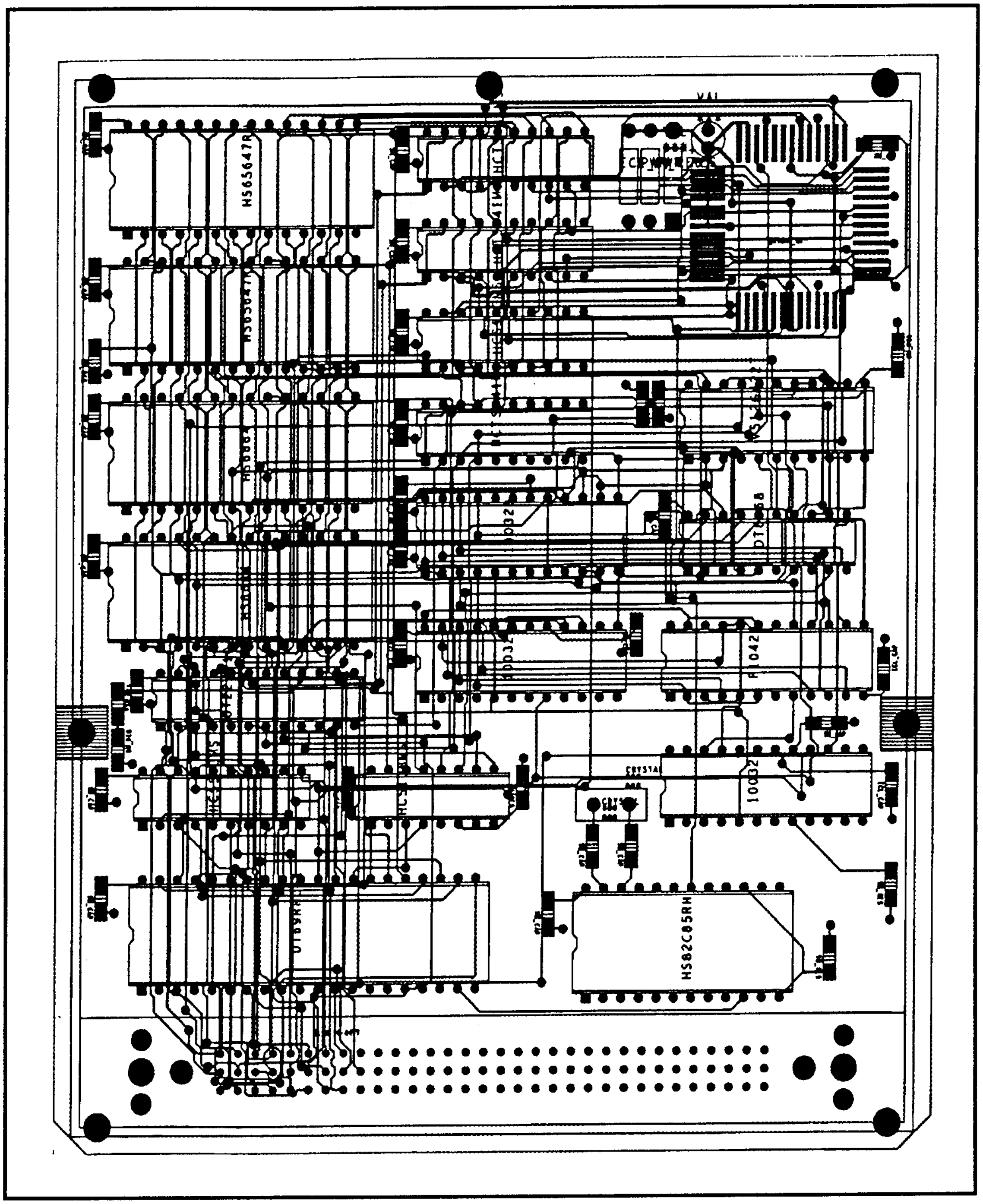


Figure 14: Top And Bottom Routing On Daughterboard

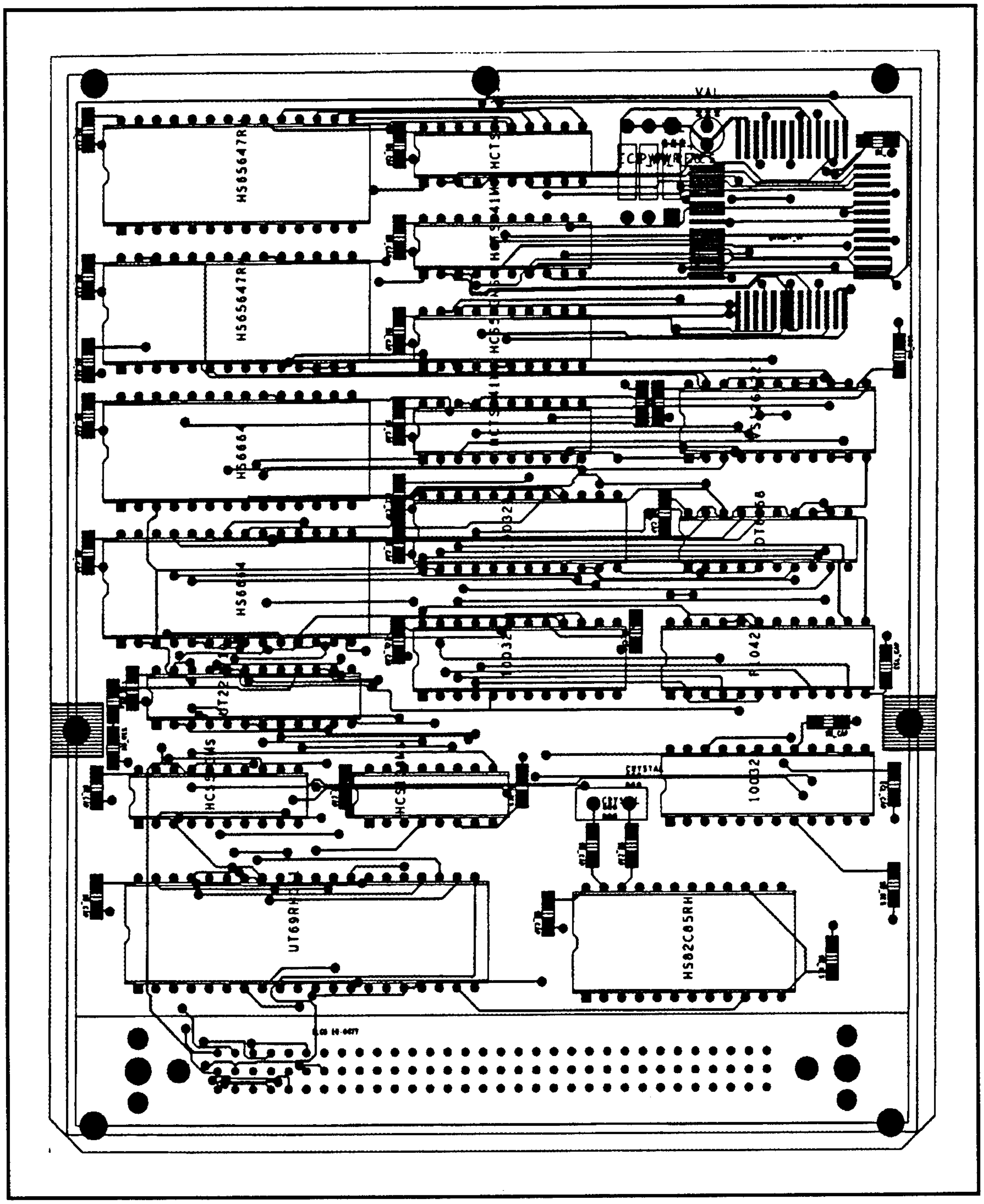


Figure 15: Top Layer Routing

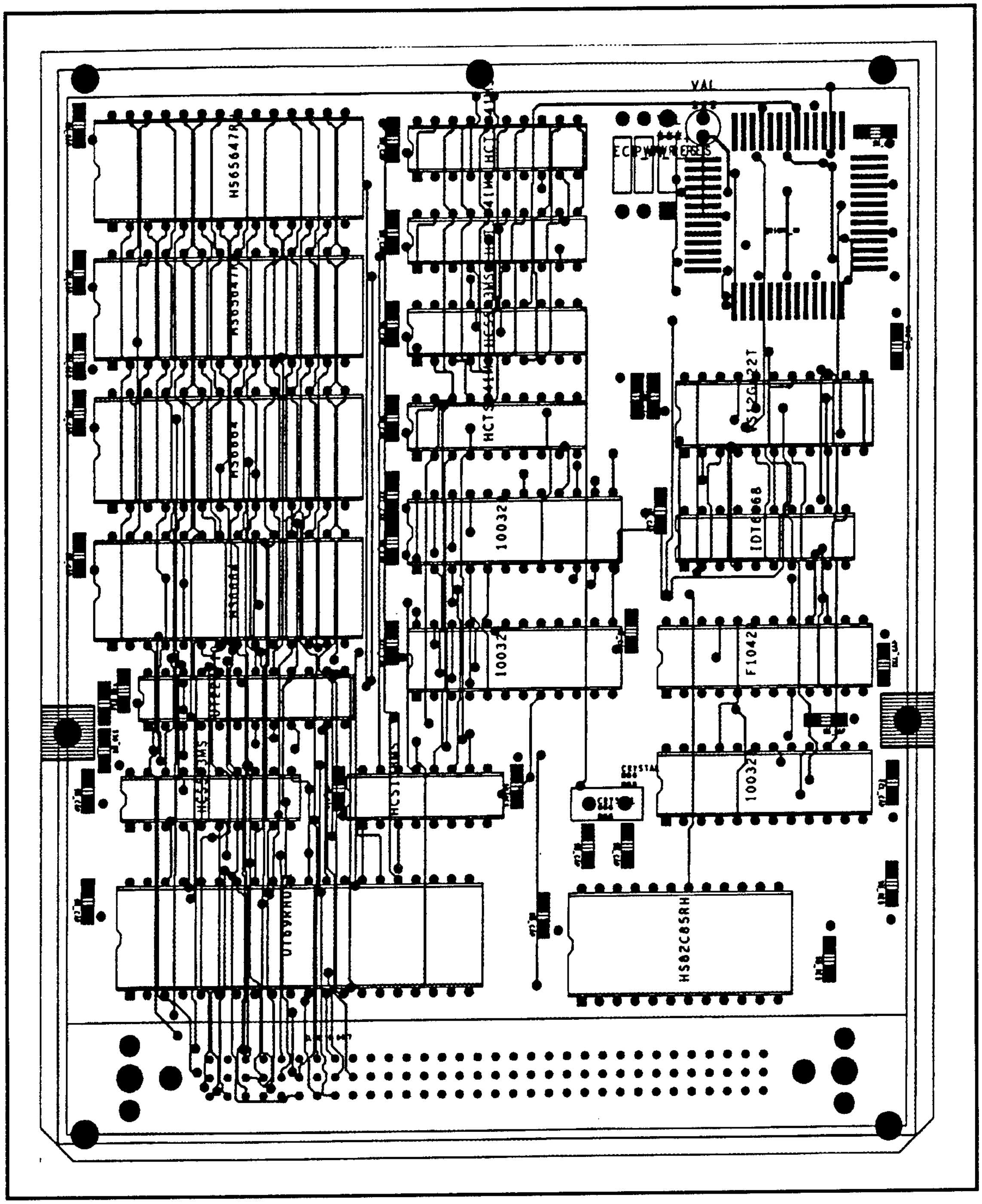


Figure 16: Bottom Layer Routing

5. Creating Output

At this point, the design is ready to create the NCDRILL and NCROUTE files. These text files contain coordinates for all holes to be drilled and information on cutting out the circuit board shape. A copy of the output files for the daughterboard design is included in Appendix B. With this information, a printed circuit board fabricator has the necessary information to build the board to design specifications. This completes the daughterboard design.

VII. CONCLUSIONS

A. DESIGN CONCLUSIONS

The daughterboard design will provide an excellent method for gauging orbital radiation effects. The radiation hardened components will provide a stable mechanism to evaluate the 'XGaAs IC and three different logic families of SRAM. During the design process, the Cadence Design Software proved to be an effective tool on developing the circuit board design. Cadence provides useful tools for all aspects of the design process, from library development to physical layout. Because of the flexibility of Cadence, future modifications to the design could incorporate a 32 bit microcontroller, a faster bus speed, larger memories, and follow-on versions of the 'XGaAs IC.

B. BOARD FABRICATION

Many PCB fabricators should be able to utilize the Cadence output files to create the PCB. One nearby fabricator who has worked with NPS is West Coast Circuits in Watsonville, CA (408) 728-4271.

C. COMPONENT COST

Table 4 below summarizes the cost of the individual components.

Component	Cost ($)	Distributor	Phone
UT69RH051	2500	UTMC	(805) 445-6665
UT22VP10	1800	UTMC	(805) 445-6665
HS-6664RH	2000	Ewing Foley	(408) 342-1220
HS-65647RH	1590	Ewing Foley	(408) 342-1220
HS-82C85RH	1350	Ewing Foley	(408) 342-1220
HCS138MS	209	Ewing Foley	(408) 342-1220
HCS573MS	215	Ewing Foley	(408) 342-1220
HCTS541MS	215	Ewing Foley	(408) 342-1220
VS12G422T	n/a	n/a	n/a
IDT6168	15	IDT	(408) 943-9270
F10422	22	Future Electronics	(408) 433-0822
100328	250	Future Electronics	(408) 433-0822

Table 4: Component Cost

D. PROGRAMMING & TESTING

Software for the daughterboard will have to be developed from the MCS51 programming language. Extensive documentation is available in the Intel Microcontroller Handbook. Once the software is written, it will need to be "burned" into the HS-6664RH PROMs. A possible consideration to troubleshoot the daughterboard would be to design a circuit board to mimic the daughterboard panel controller. Access to the daughterboard is available via the ELCO connector. The female opposite of the connector could be connected to the HP 64000 analyzer units to simulate the EPC.

When the UT22VP10 is purchased, the IC will need to be burned-in. Figure 11 depicts a summary of the logic. Sum-of-products equations can be easily generated for this device. For instance, the AND function combining the PSEN* and RD* signals of the '8051 microcontroller would be defined as follows:

$$I/O7 = I4 * I5 \qquad \text{Equation 7.1}$$

I/O7 corresponds to output pin 7 on the UT22VP10, I4 and I5 correspond to input pins 4 and 5. By connecting I4 and I5 to PSEN* and RD*, respectively, the output of I/O7 will be the desired product of the two input signals.

Radiation hardened components are expensive and generally require several months to order from the manufacturer. However, for the purposes of testing the design, it would be beneficial to construct a second daughterboard with commercial components, that is non-radiation hardened components. These components are widely available, are logically equivalent and have the same pin-out as their radiation hardened counterparts, and cost less than a few dollars each. Building a second board would also provide the Experimental GaAs IC

E. SUMMARY

The daughterboard design is a remarkable testament to demonstrating the skills one has acquired in graduate education. This design project completes several months of component familiarization and evaluation, CAD tool familiarization, and application of electrical engineering theory. At this point, the daughterboard is ready to be fabricated and components may be ordered. Possible changes to the Experimental GaAs IC, which is still in the design phase, may necessitate minor changes to the daughterboard design.

LIST OF REFERENCES

1. Sedra & Smith, *Microelectronic Circuits*, 3rd Edition, Saunders College Publishing, Philadelphia, PA, 1991.
2. *"Microelectronics and Photonics Test Bed (MPTB) Experiment Daughterboard Interface Control Document"*, Revision D, Dec. 8, 1995.
3. LaBel, Kenneth A., Gates, Michele M., Moran, Amy K., *Commercial Microelectronics Technologies for Applications in the Satellite Radiation Environment*, http://flick.gsfc.nasa.gov/radhome/papers/aspen.htm, 1995.
4. Wakerly, John F., *Digital Design Principles and Practices*, 2nd Edition, Prentice Hall Publishing, Englewood Cliffs, NJ, 1994.
5. Clements, Alan, *Microprocessor System Design*, Second Edition, PWS Publishing, Boston, 1992.
6. Rapid Part Reference Manual v. 1.4, Cadence Openbook Online Help, Cadence Design Systems, 1996.
7. Concept Schematic User Guide, v. 1.6, Cadence Openbook Online Help, Cadence Design Systems, 1996.
8. Allegro User Guide, Volumes 1-7, Cadence Openbook Online Help, Cadence Design Systems, 1996.
9. *Intel Microcontroller Handbook*, Volume1, Intel Corporation, 1992.

APPENDIX A. MPTB INTERFACE CONTROL DOCUMENT

The following pages contain the MPTB Interface Control Document, Revision D Draft, December 8, 1995.

MICROELECTRONICS
AND
PHOTONICS
TEST BED (MPTB)
EXPERIMENT DAUGHTERBOARD
INTERFACE CONTROL
DOCUMENT (ICD)

REVISION D
DRAFT
DECEMBER 8, 1995

1.0 SCOPE

1.1 SCOPE

This Interface Control Document (ICD) defines and controls the design at the interface between daughterboard and motherboard on each Experiment Panel of the Microelectronics and Photonics Test Bed (MPTB). This ICD is intended to ensure compatibility between daughterboard and motherboard by documenting form, fit, and functional interface agreements required to satisfy design, test, and integration.

1.2 MPTB MISSION DEFINITION

The Microelectronics and Photonics Test Bed (MPTB) is a satellite payload that will be used to measure the effects of space radiation on microelectronic and photonic devices and subsystems. Functional electronics changes caused by ionizing particles and total-dose radiation will be measured in a controlled experiment, with device data telemetered to the ground. The following effects will be measured: single event upsets, single event latchup, bit error rate effects, timing degradation, threshold voltage shifts, leakage current increases, and functional failure.

1.3 INTERFACE ITEM DESCRIPTION

1.3.1 <u>MPTB Experiment Description</u>. MPTB consists of a redundant Core Electronics Unit (CEU), and three experiment panels, each up to eight daughterboard slots. A block diagram is shown in Figure 1.

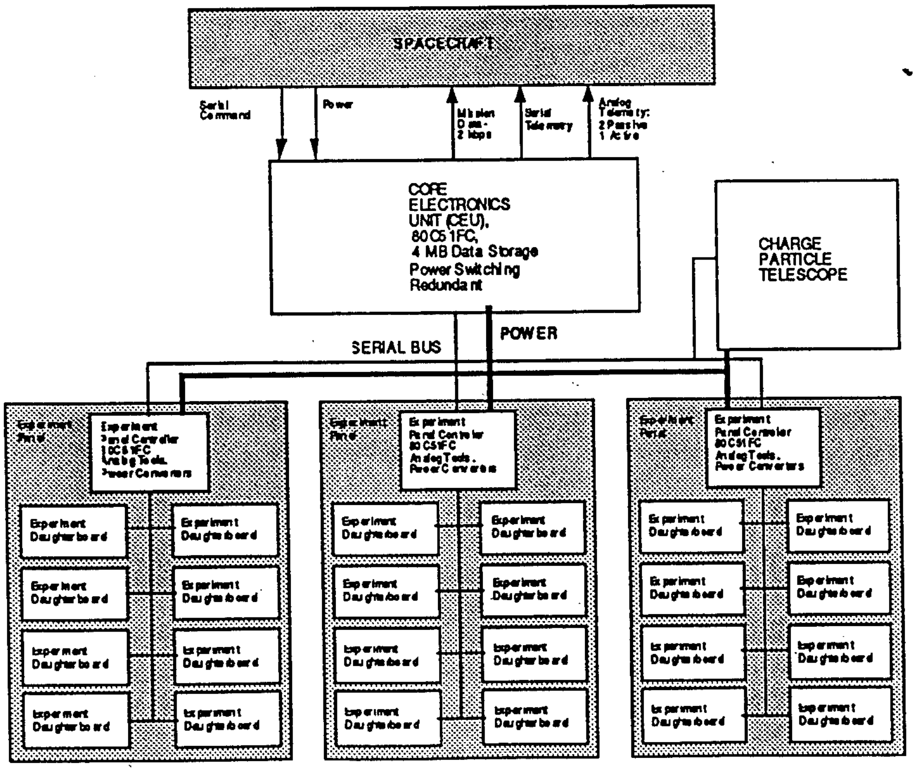


Figure 1 - MPTB Block Diagram

1.3.2 Experiment Panel Description. An experiment panel consists of an 80C51 microcontroller, analog measurement tools, power supplies, and up to eight daughterboards as shown in Figure 2.

1.3.3 Daughterboards. A daughterboard contains an individual microelectronics of photonics experiment along with the circuitry necessary to interface with the experiment panel motherboard interface.

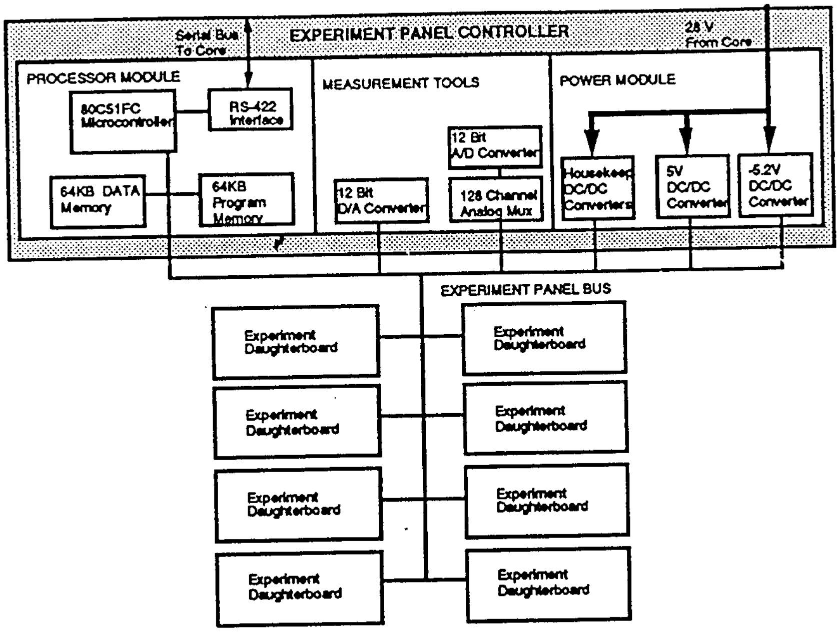


Figure 2 - Experiment Panel Block Diagram

2.0 APPLICABLE DOCUMENTS

The following documents of the issue specified contribute to the definition of the experiment /space interface and form a part of this document to the extent specified herein. Where requirements of the referenced documents differ from those requirements stated herein, the requirements specified herein have precedence.

2.1 GOVERNMENT DOCUMENTS

Military Documents	Title
MIL-STD-461C 4 Aug 86 Notice 1 1 Apr 87 Notice 2 15 Oct 87	Electromagnetic Emission and Susceptibility Requirements for the Control of Electromagnetic Interference
MIL-STD-1540B	Test Requirements for Space Vehicles

(USAF)
10 Oct 82
Notice 1, 31 Jul 89
Notice 2, 8 Feb 91
Notice 3, Feb 12 91

MIL-STD-1541A (USAF) 30 Dec 87	Electromagnetic Compatibility Requirements for Space Systems

2.2 NON-GOVERNMENT DOCUMENTS

INTEL 270646	Embedded Microcontrollers

3.0 DAUGHTERBOARD REQUIREMENTS

3.1 STRUCTURAL AND MECHANICAL REQUIREMENTS

3.1.1 Board Configuration and Envelope

3.1.1.1 Single Slot Board Configuration and Envelope The configuration and envelope of a single slot double-sided daughterboard is shown in Figure 3.

3.1.1.2 Double Slot Board Configuration and Envelope The configuration and envelope of a double slot double-sided daughterboard is shown in Figure 4.

3.1.3 Mass Properties

3.1.3 Single Board Configuration Mass Properties The total weight of a single slot MPTB daughterboard shall not exceed 0.5 pounds (227 grams). This weight includes the VME connector, mounting screws, and any stiffeners that are required.

3.1.3 Double Board Configuration Mass Properties The total weight of a double slot MPTB daughterboard shall not exceed 1 pound (454 grams). This weight includes the VME connectors, mounting screws, and any stiffeners that are required.

3.1.4 Connector Physical The daughterboard/motherboard interface requires 3-row, 96 pin inverted male DIN connectors (#ELCO 10-8477-096-002-904, military part number M55302/157-02) for the daughterboard, and 3-row, 96 pin, straight-thru, female DIN connectors(#ELCO 20-8457-096-002-908, military part number M55302/132-01). A mechanical drawing of the connector is on the following page.

3.1.5 Materials Selection All materials exposed to the environment shall meet NASA Specification SP-R-0022 with less than 1.0% TML and less than 0.1% CVCM.

3.2 ELECTRICAL INTERFACE

3.2.1 Voltages. Each daughterboard will be provided switched +5V, -5.2V, and +/-15V. All voltages are +/- 5%. The output ripple in a 2 Mhz bandwidth at full load for each of the power supplies is shown in the table below.

Power Supply Output Voltage	Peak to Peak Output Voltage Level
+5V	80 mV
-5.2V	65 mV
+/-15V	30 mV

3.2.2 Grounding.

3.2.2.1 GND. This is signal ground, which is the return for the +5V and the -5.2V supplies.

3.2.2.2 ANA_RTN. This is return for the +/-15V supplies.

3.3.2.3 Ground Isolation. ANA_RTN must be isolated by at least 100 KOhms from GND. Additionally, both ANA_RTN and GDN must be isolated by atleast 1 MOhm from the chassis ground (tie in points on board, thermal conductance strip, and keep out area around board will be tied to chassis ground.).

3.2.2 Power.

3.2.2.1 Single Board Configuration Power. The maximum power used by any single slot daughterboard shall not exceed 10 Watts. The orbital average power for each daughterboard will be approximately 2 Watts.

3.2.2.2 Double Board Configuration Power. The maximum power used by any double slot daughterboard shall not exceed 20 Watts. The orbital average power for each double slot daughterboard will be approximately 4 Watts.

3.2.3 Low Power Option.

3.2.3 Single Board Configuration Low Power Option. If a single slot daughterboard is to be biased at all times (for a total dose experiment), the daughterboard shall have a low power mode that shall not exceed 0.5 Watts.

3.2.3 Double Board Configuration Low Power Option. If a double slot daughterboard is to be biased at all times (for a total dose experiment), the daughterboard shall have a low power mode that shall not exceed 1 Watt.

3.2.4 Connector Pin-out.

3.2.4.1 Single Slot Connector Pin-out. Sinlge slot daughterboard pin assignments are shown on the following page. The pin locations are referenced to the daughterboard connector.

Pin	Row A	Row B	Row C
1	ADDR0	ADDR7	DATA0
2	ADDR1	ADDR8	DATA1
3	ADDR2	ADDR9	DATA2
4	ADDR3	ADDR10	DATA3
5	ADDR4	RD*	DATA4
6	ADDR5	WR*	DATA5
7	ADDR6	INT*	DATA6
8	BD_SEL*	INT*_RESET*	DATA7
9	unassigned	RESET*	unassigned
10	GND	GND	GND
11	GND	GND	GND
12	+5V	+5V	+5V
13	+5V	+5V	+5V
14	+5V	+5V	+5V
15	GND	GND	GND
16	GND	GND	GND
17	-5.2V	-5.2V	-5.2V
18	-5.2V	-5.2V	-5.2V
19	-5.2V	-5.2V	-5.2V
20	GND	GND	GND
21	GND	GND	GND
22	+15V	+15V	+15V
23	-15V	-15V	-15V
24	ANA_RTN	ANA_RTN	ANA_RTN
25	ANA_RTN	ANA_RTN	D/A_REF_RTN
26	ANALOG1	ANA_ RTN_SENSE	D/A_V
27	ANALOG2	ANALOG7	ANALOG12
28	ANALOG3	ANALOG8	ANALOG13
29	ANALOG4	ANALOG9	ANALOG14
30	ANALOG5	ANALOG10	Dosimeter_G
31	ANALOG6	ANALOG11	Dosimeter_S
32	Temp_sense_High	Temp_sense_Rtn	Dosimeter_D

3.2.4.2 Double Slot Connector Pin-out. A double slot daughterboard will contain two independent single slot connectors.

3.2.5 Digital Interface.

3.2.5.1 Single Slot Digital Interface and Schematic. The digital interface between the motherboard and a single slot daughterboard will use Harris HCS245 transceivers. This interface circuitry resides on the motherboard. A schematic is shown in Figure 5. The signals on the left side of the schematic come from the controller. The signals on the right side of the schematic are connected to the 96 pin DIN connector for the daughterboard. Note that the signals on the right side of the schematic are tri-stated unless that daughterboard is selected.

3.2.5.2 Double Slot Digital Interface. The digital interface between the motherboard and a dougle slot daughterboards will consist of two independent single slot digital interface circuits shown in Figure 5.

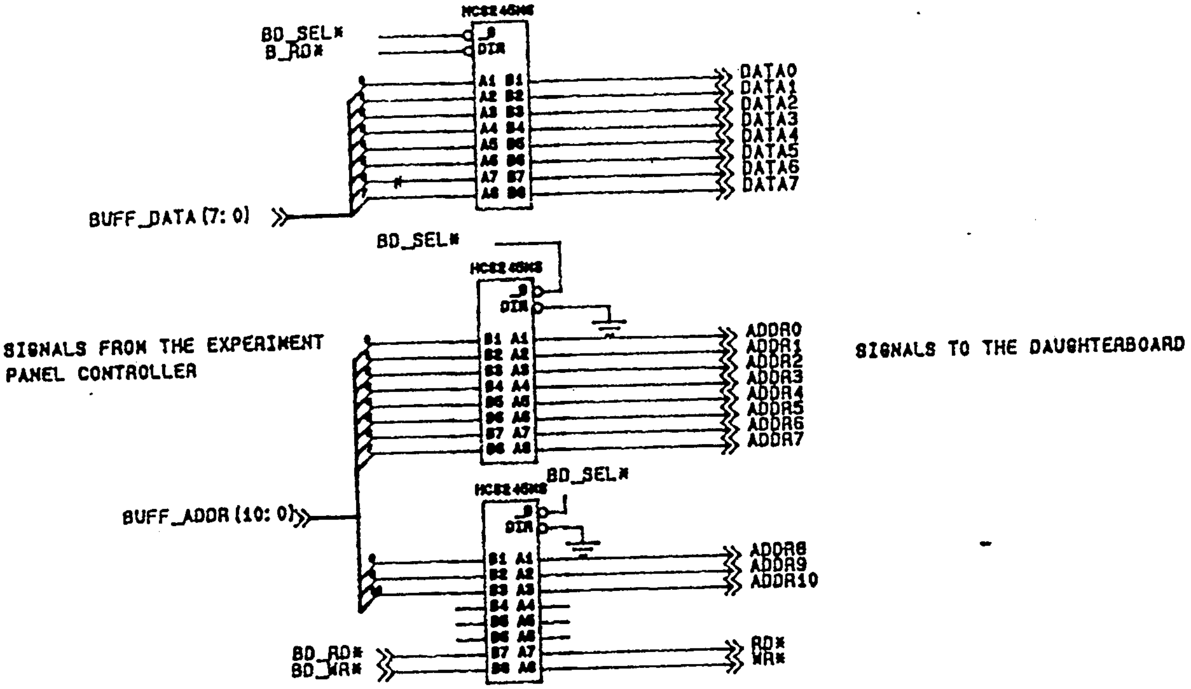


Figure 5 - Interface Circuitry

3.2.7 Analog Measurement Interface.

3.2.7.1 Single Slot Analog Measurement Interface. The analog interface will consist of 14 analog lines and one analog return line (ANA_RTN_SENSE). The voltage measurement range will be between -4 and 6.24 Volts, differentially measured between ANALOGn (n is from 1 to 14) and ANA_RTN_SENSE. The measurement resolution is 2.5 mV.

3.2.7.2 Analog Measurement Interface. The analog interface will consist of 28 analog lines and two analog return lines. The voltage measurement range will be between -4 and 6.24 Volts. The measurement resolution is 2.5 mV.

3.2.7.3 Current Sensing Circuitry. The recommended current sensing circuitry is shown in Figure 6.

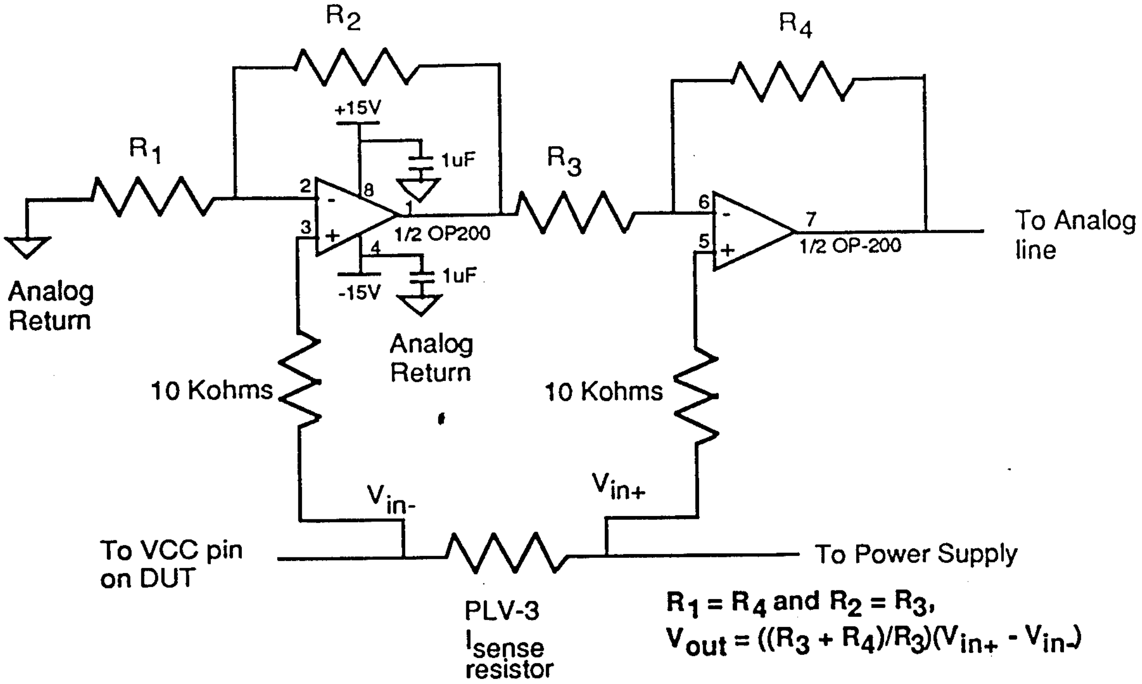


Figure 6 - Current Sensing Circuitry

3.2.7.4 Temperature Sensing Circuitry. The temperature sensing circruitry is shown in Figure 7. The AD590 will be provided by NRL. The AD590 is in a 2-pin flatpack package shown on the following page.

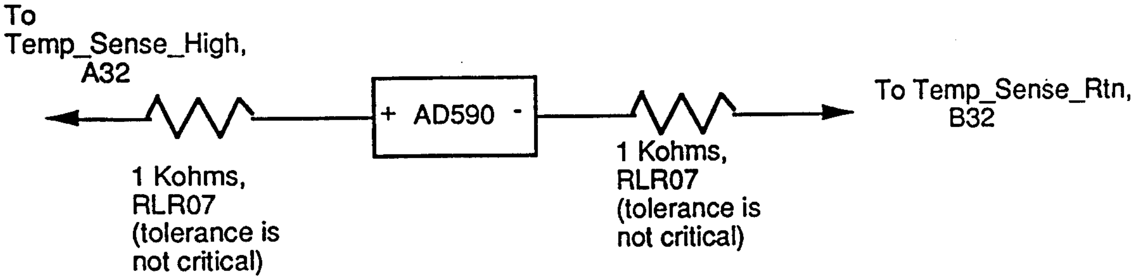


Figure 7 - Temperature Sensing Circuitry

3.2.7.5 Dosimeter Circuit. The dosimeter circuit is shown in Figure 8. The dosimeter will be provided by NRL. The dosimeter is in an 8-pin TO-5 (TO-99) package. The mechanical drawing is on the page following the 2-pin flatpack.

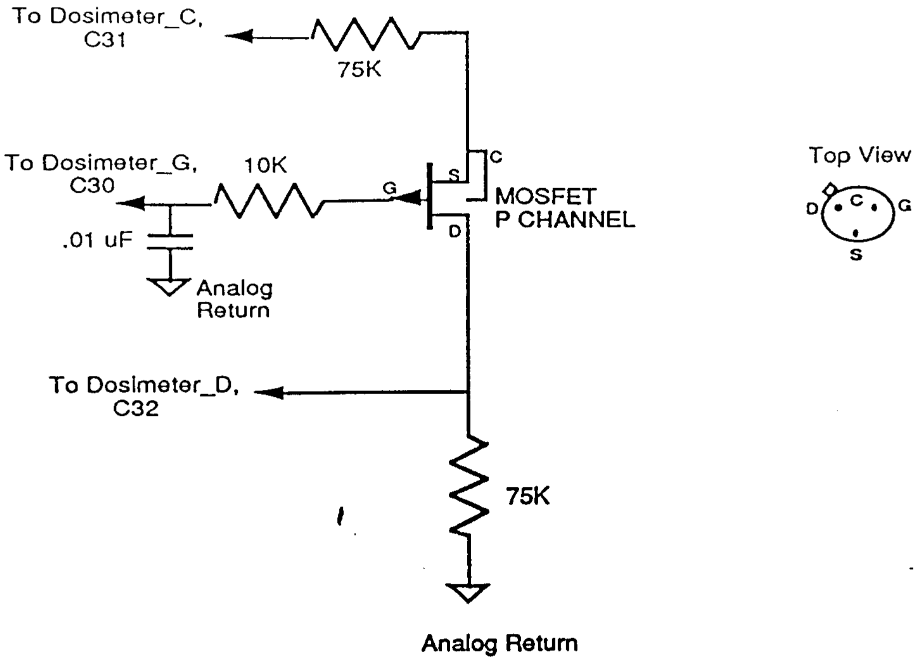


Figure 8 - Dosimeter Circuitry

3.2.8 Digital to Analog Interface.

3.2.8.1 Single Slot Digital to Analog Interface. A single slot daughterboard will have a single digital to analog interface with a voltage range between -4 and 6.24 volts referenced differentially between signals D/A_V (pin C26) and D/A_REF_RTN (C25). Daughterboards using these signals shall provide a minimum of 1 Megaohm input impedance on each signal. The voltage is from a 12-bit D/A converter, the Analog Devices AD565ATD. The voltage resolution is 2.5 mV.

3.2.8.2 Double Slot Digital to Analog Interface. A double slot daughterboard will have two independent digital to analog interfaces as described in 3.2.8.1. These two interfaces are independently switched; when one is on, the other will be off. They can both be off at the same time though.

3.2.9 Electromagnetic Compatibility. The daughterboard shall pass the CE01 and CE03 tests with connected to a Line Impedance and Source Network that simulates the Experiment Panel's power outputs. The test levels shall follow CE01 and CE03, except the initial value is based on -40dB of the maximum normal operating load current. The MPTB experiment must meet the EMI requirements set in Figures 9 and 10. The MPTB designers will work with the individual experimenter designers to insure compatibility at the daughterboard level.

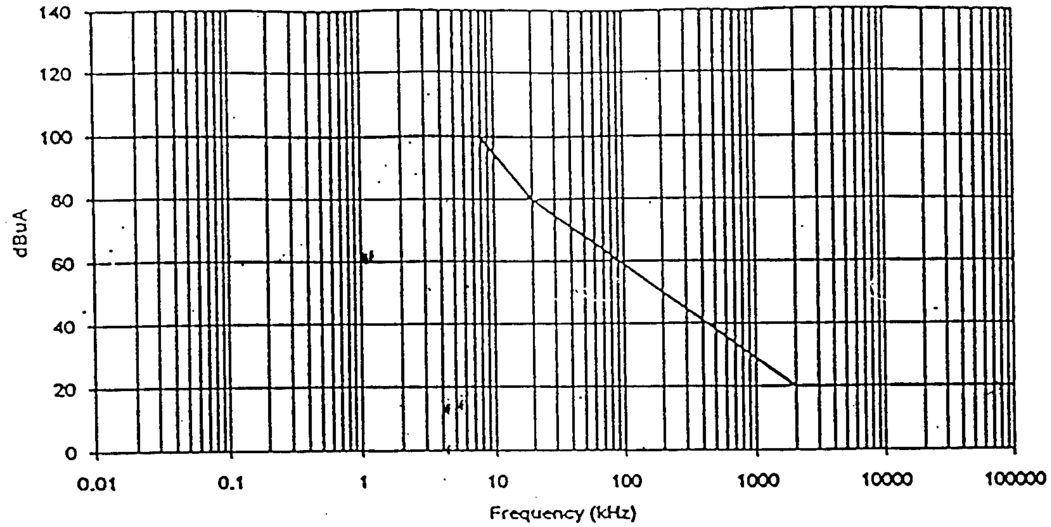


Figure 9 - Narrowband Conducted Emissions Limit

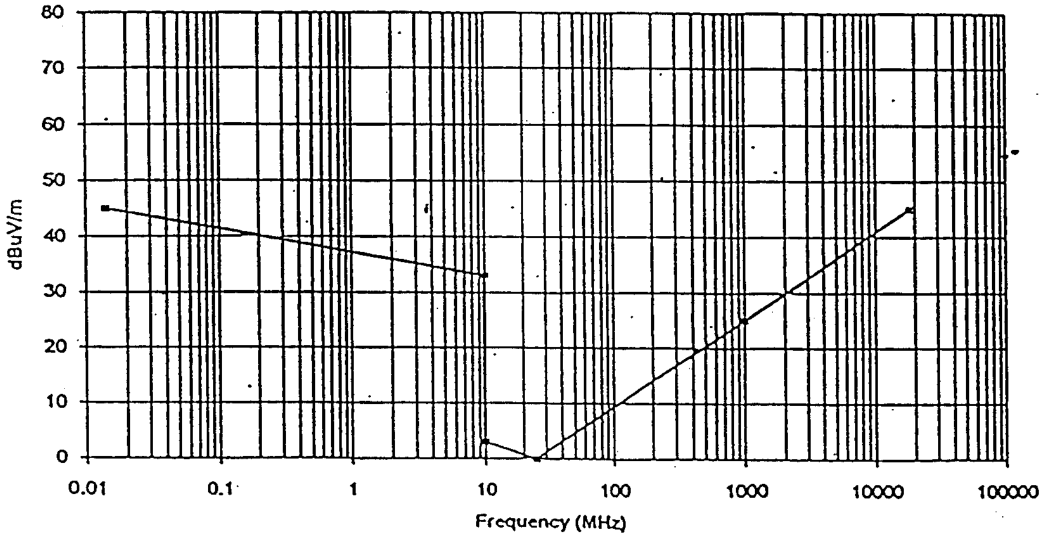


Figure 10 - Narrowband Radiated Emissions Limit

3.3 SIGNAL INTERFACE

This section defines signal interfaces between the 8051 microcontroller on the experiment panel and the daughterboards.

3.3.1 RD*. An 8051 external data read cycle. The 8051 is running at 12 Mhz. Read cycle timing is shown in Figure 11.

3.3.2 WR* An 8051 external data write cycle. The 8051 is running at 12 Mhz. Write cycle timing is shown in Figure 12.

3.3.3 INT*. The daughterboard can pull this line low interrupt the processor. This tells the processor that the daughterboard has data to pass on. The daughterboard shall not modify this data until this line is reset.

3.3.4 INT*_RESET*. This signal is driven low by the processor to reset a daughterboard's INT* line. This will be done after the processor has read all the necessary information from the daughterboard. The INT*_RESET* line will remain low until the daughterboard's INT* returns to a high logic level.

3.3.5 BDSEL*. This signal is driven low when the particular daughterboard is selected. After the falling edge, the daughterboard will have no more than 657 nanoseconds before it must give the panel controller full control of any shared memory. When BDSEL* returns high, the daughterboard may resume control of any shared memory.

3.3.6 RESET*. This signal is driven low to reset the daughterboards.

3.4 SOFTWARE INTERFACE

3.4.1 Overview The Digital Interface between the Experiment Panel Controller (EPP) and the various experiments (DUTs) is done completely in a 2k section of the EPP's data memory. (One 2k section of EPP memory for each DUT) The EPP will need to send commands and collect error messages from the DUTs. This section discusses the way this digital information is passed between the EPP and the DUTs. There are additional resources, that are not discussed in this section of the document, for the exchange of analog data between the EPP and the DUTs . MPTB also has a goal of DUT modularity, that is if a particular DUT is unavailable or a more important DUT is found the new board can be plugged right in to the old slot with little impact. To achieve this goal Flight Software will be supporting two standard interfaces.

3.4.2. Type I Interface: Fixed, Simple Interface This interface type is designed for experiments that require very basic start/stop commands and/or will generate the same error message every time. Both the command and the telemetry Type I interfaces will have fixed locations for all input and output. Due to its generality, there may be bytes that are not used by a particular experiment. Each experiment will have the option of using either the Type I command interface or the Type I telemetry interface or both interfaces.

3.4.2.1 Type I Command Interface The Command Interface for Type I DUTs will start at location 0x000 of the 2k memory mapped interface. The interface will be the same for all Type I DUTs. Figure 13 shows the command interface. The Command Byte of the interface is used to both indicate that a command is present and what that command is. All other command data are written prior to writing the command byte.

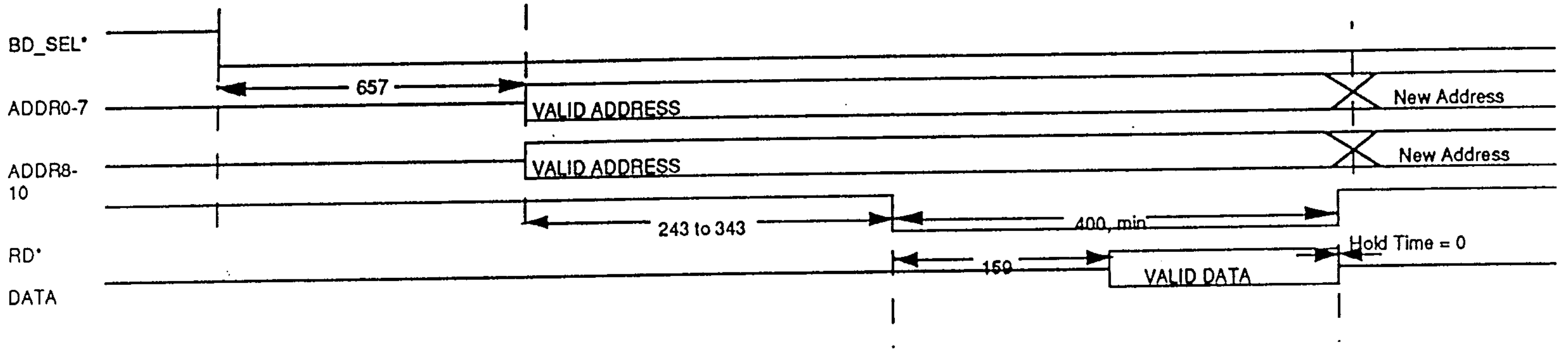


FIGURE 11 - Read Cycle Timing

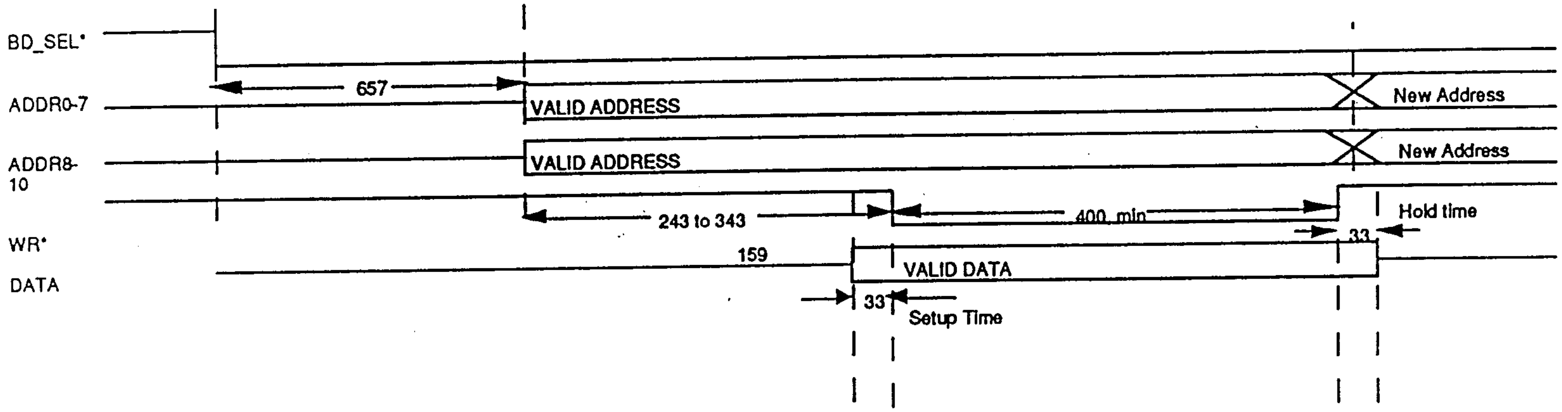


FIGURE 12 - Write Cycle Timing

0x000	Command
001	MSB of Start Addr
002	Start Addr
003	Start Addr
004	LSB of Start Addr
005	MSB of Stop Addr
006	Stop Addr
007	Stop Addr
008	LSB of Stop Addr
009	MSB of Pattern Data
00A	Pattern Data
00B	Pattern Data
00C	LSB of Pattern Data
00D	MSB of Refresh Rate
00E	LSB of Refresh Rate
	RESERVED...

Figure 13: Type I Command Interface

A command of zero (0x00) will be used to stop the current experiment during execution. Typically a memory experiment would need a start address (up to 32 bits) and a stop address (up to 32 bits) over which the particular test will run. It would also need the data pattern (up to 32 bits) to write for this test. For those experiments requiring a refresh rate a 16 bit location is available. The locations for each data item will be the same for ALL users of this interface. If an experiment needs less than 32 bits of addressing, it will still find the start address at 0x001 and the stop address at 0x005. This interface is primarily for memory experiments although any experiment desiring a simple interface may use the data in the above locations in any way suitable to the experiment.

3.4.2.2 Type I Telemetry Interface The Telemetry Interface for Type I DUTs will start at location 0x110 of the 2k memory mapped interface. The interface will be the same for all Type I DUTs. Figure 14 shows the Telemetry interface. All bytes, including the counter bytes, are collected whenever the DUT asserts the interrupt line. The counter bytes are intended to be used in a solar flare scenario. In such a situation, the experiment would just scan its DUT and rather than report details on each error, it would just count all errors and periodically assert the interrupt line. In all modes the experiment would stop once it asserts the interrupt line and resume only after the EPP collects its data and clears the interrupt. The interrupt line, when asserted by a DUT, triggers a time stamp that is stored with the data the EPP collects from the DUTs. The labels in Fig. 14 were assigned with a memory experiment in mind, as long as a DUT ALWAYS uses the same location for a specific item any data may be put in any location with the exception of the counter bytes that must be used as counter or not used.

0x110	MSB of Error Addr
111	Error Addr
112	Error Addr
113	LSB of Error Addr
114	MSB of Read Data
115	Read Data
116	Read Data
117	LSB of Read Data
118	MSB of Written Data
119	Written Data
11A	Written Data
11B	LSB of Written Data
11C	MSB of Counter 1
11D	LSB of Counter 1
11E	MSB of Counter 2
11F	LSB of Counter 2
120	MSB of Counter 3
121	LSB of Counter 3
122	RESERVED...
123	RESERVED...

Figure 14: Type I Telemetry Interface

3.4.3 Type II Interface: Variable, Packet Oriented Interface This interface type is designed for experiments that require more complex commands and/or will generate more complex or variable error messages. Both the command and the telemetry Type II interface will have variable length areas for all input and output. The EPP, for commanding, and the DUT, for telemetry messages, will be responsible for using a byte count to give the length of the command/telemetry message. Each experiment will have the option of using either the Type II command interface or the Type II telemetry interface or both interfaces.

3.4.3.1 Type II Command Interface The Command Interface for Type II DUTs will start at 0x000 of the 2k memory mapped interface. The EPP and the DUT must use the software semaphore (location 0x000) to synchronize the passing of data. IMMEDIATELY upon startup the DUT MUST give the semaphore. (write 0xC3 to location 0x0000) The EPP will write the new command data, including the byte count, then set the semaphore to indicate a new command is ready. (write 0x3C to location 0x0000) Upon detecting the semaphore set for a new command, the DUT reads the byte count, followed by reading the command data. After it has collected the current command, the DUT sets the semaphore to indicate it has read the command. (write 0xC3 to location 0x0000) As indicated in Fig.15, any command may contain up to 255 bytes of actual data.

0x000	Software Semaphore
001	Command Byte Count
002	Byte 1 of CMD Data
	...Bytes 2 - 254...
100	Byte 255 of CMD Data
	RESERVED...

Figure 15: Type II Command Interface

3.4.3.2 <u>Type II Telemetry Interface</u> The Telemetry Interface for Type II DUTs will start at location 0x110 of the 2k memory mapped interface. The communication synchronization will be accomplished by the interrupt line. When the DUT has data for the EPP to collect, it will assert the interrupt line. The EPP will then collect the data stored in the DUTs telemetry area. No additional data may be written by the DUT until the EPP clears the interrupt indicating it has read all the data. Due to downlink formatting the TLM data will be limited to 242 bytes of data per interrupt (see Figure 16).

0x110	TLM Byte Count
111	Byte 1 of TLM Data
	...Bytes 2 - 241...
202	Byte 242 of TLM Data
203	RESERVED...

Figure 16: Type II Telemetry Interface

3.5 THERMAL

3.5.1 <u>Heat Dissipation</u>. The daughterboard shall have the ability to dissipate enough heat such that, at maximum power, the temperature does not exceed the maximum operating junction temperature.

3.5.2 <u>Operating temperature range.</u> The operating temperature range is -10C to +50C.

3.5.3 <u>Survival temperature range.</u> The survival temperature range is -40C to +60C.

3.6 FLIGHT ENVIRONMENT

The following parameters represent the induced flight environments to which the interfacing experiment is exposed during ascent and earth orbit. The experiment is expected to survive and/or operate when exposed to any feasible combination of those parameters encountered from ascent through mission operation.

3.6.1 <u>Acoustic</u>. Maximum expected flight acoustic environment at the MPTB interface with the host vehicle is shown in Figure 17.

1/3 Octave Band Center Frequency (Hz)	Sound Pressure Level (dB)
32	120.7
40	122.3
50	125.0
63	126.5
80	127.5
100	129.0
125	130.0
160	130.5
200	131.0
250	131.5
315	128.0
400	126.0
500	124.0
630	122.0
800	120.0
1000	118.0
1250	116.5
1600	114.5
2000	113.0
2500	111.5
3150	110.0
4000	108.5
5000	107.0
6300	106.0
8000	105.5
10000	105.0
Overall	139.5

Figure 17 - Acoustic Environment

3.6.2 Vibration. Maximum predicted launch vibration levels for the at the MPTB interface with the host vehicle are shown in Figure 18.

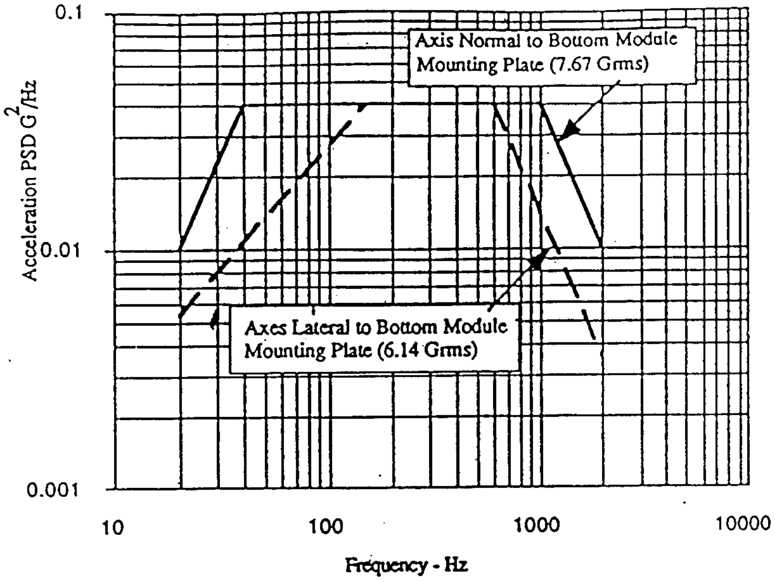


Figure 18 - Maximum Expected Launch Vibration Levels

3.6.3. Shock. The predicted pryro-shock levels at the MPTB interface with the host vehicle are shown in Figure 19.

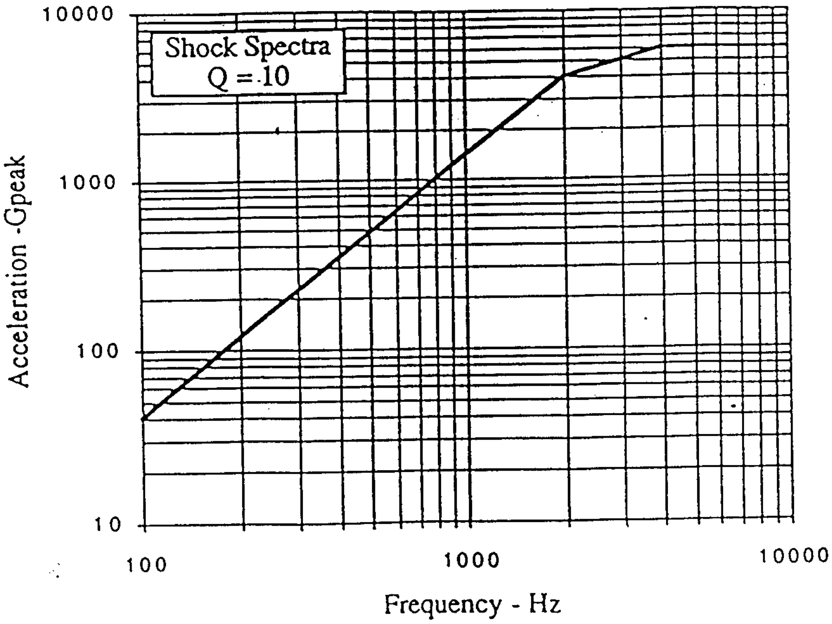


Figure 19 - Maximum Expected Pyro-shock Levels

5.0 TEST

The MPTB daughterboard will undergo environmental and functional testing at NRL after integration into the experiment panels.

5.1 PRE-INTEGRATION TESTS

5.1.1 Visual Inspection. Each flight daughterboard will be visually inspected for flight worthiness.

5.1.2 Physical Properties Inspected. Each flight daughterboard will be measured and weighed to insure that it falls within the defined envelope and weight.

5.1.2 Interface Verification Test. Each daughterboard will be inserted into a test experiment panel motherboard to test out its interfaces.

5.1.2.1 Digital Interface Test. The waveforms described in Section 3.3 will be tested. Data set up and hold times will be measured.

5.2 POST-INTEGRATION TESTS

5.2.1 Tests Performed at NRL.

5.2.1.1 Test Performed on the Engineering Model - Qual Level Test

1. Random vibration at flight level +6dB, 3 axes for 3 minutes each
2. Acoustic at flight level +6dB for 2 minutes
3. Flight shock level, 3 axes, 3 shocks each
4. Thermal Cycle: -20C to +60C, 9 cycles
5. EMI testing

5.2.1.2 Test Performed on the Flight Unit

1. Random vibration at flight level, 3 axes for 1 minute each
2. Acoustic at flight level for 1 minute
3. Flight shock level, 3 axes, 1 shock each
4. Thermal Cycle: -10C to +50C, 9 cycles at box level
5. Thermal Vacuum: -10C to +50C, 3 cycles at system level
6. EMI testing

6.0 ACCEPTANCE CRITERIA

To be accepted as a candidate flight board for the USA experiment, a daughterboard must meet the following criteria:

1. NRL review during PDR and CDR.
2. Delivery of engineering model prior to qualification testing.
3. Delivery of flight daughterboard before final integration and test.
4. Satisfactorily complete pre-integration testing.
5. Satisfactorily complete environmental testing.

6.1 Deliverables

1. Engineering Model.
2. Flight daughterboard.
3. Full board schematic.
4. List of discrete analog input and outputs.
5. Command and digital data interface description.
5. Documentation describing board functions.

APPENDIX - SUGGESTED INTERFACE DEVELOPMENT TOOLS

The flight software on MPTB will be developed using Nohau's *Emul51-PC* emulation hardware, Chip Tools's Simulator and Debugger, and Franklin Software's *C51* compiler and A51 assembler. The processor is an 8051FC running at 12 Mhz. These tools will be hosted on a PC running DOS and Windows 3.1. The ONLY interface to the daughterboards from the EPP is through the memory mapped interface. Data into and out of the daughterboards will be done as described in Section 3.4 of this document. Replication of the circuitry in Figure 5 would be desirable to emulate the hardware interface. The BD_SEL* line can be generated by decoding the upper 5 bits of the 8051 address bus to memory map the daughterboard's 2K memory location into the upper 16K locations in the 8051's memory map.

APPENDIX B. NCDRILL AND NCROUTE FILES

The outputs below are a print out of the NCDRILL and NCROUTE tape files.

A. NCDRILL FILE

```
;LEADER: 12
;HEADER:
;CODE  : ASCII
;FILE  : ncdrill1 for layers TOP and BOTTOM
;Holesize 1. = 26.000000 PLATED MILS
;Holesize 2. = 28.000000 PLATED MILS
;Holesize 3. = 36.000000 PLATED MILS
;Holesize 4. = 39.000000 PLATED MILS
;Holesize 5. = 44.000000 PLATED MILS
;Holesize 6. = 45.000000 PLATED MILS
;Holesize 7. = 110.000000 PLATED MILS
;Holesize 8. = 120.000000 PLATED MILS
;Holesize 9. = 140.000000 PLATED MILS
;Holesize 10. = 150.000000 PLATED MILS
G90
X00400Y02800
R13X00100
X01700Y03400
R13X-00100
X00400Y03550
R13X00100
X01700Y04150
R13X-00100
X00400Y04300
R13X00100
X01700Y04900
R13X-00100
X00400Y05050
R13X00100
X01700Y05650
R13X-00100
X00600Y02350
R11X00100
X01700Y02650
R11X-00100
X00500Y01800
R09X00100
X01400Y02100
R09X-00100
X00500Y00900
R19X00100
X02400Y01500
R19X-00100
X01800Y01800
R07X00100
X02500Y02100
R07X-00100
X02100Y02500
R11X00100
X03200Y02900
```

```
R11X-00100
X02100Y03200
R11X00100
X03200Y03600
R11X-00100
X02100Y03800
R09X00100
X03000Y04100
R09X-00100
X02100Y04300
R09X00100
X03000Y04600
R09X-00100
X02100Y04800
R09X00100
X03000Y05100
R09X-00100
X02100Y05300
R09X00100
X03000Y05600
R09X-00100
X03030Y00840
R11X00100
X04130Y01440
R11X-00100
X03500Y01800
R11X00100
X04600Y02200
R11X-00100
X03500Y02500
R11X00100
X04600Y02900
R11X-00100
X03600Y03200
R09X00100
X04500Y03500
R09X-00100
X03600Y03800
R10X00100
X04600Y04200
R10X-00100
M00
X04250Y01940
X00800Y02000
X01570Y02320
X01640Y02620
X01740Y00930
X02100Y02250
X01200Y02250
X00790Y02690
X00760Y04010
X03880Y03970
X02800Y02170
X04360Y04230
X02780Y00930
X01480Y00860
X04150Y04030
```

```
X04000Y04030
X01370Y01930
X04300Y02020
X01430Y03460
X02740Y02050
X02580Y01960
X03840Y05200
X04170Y04740
X03830Y05070
X04170Y05200
X03530Y04500
X03630Y03050
X03500Y03050
X01270Y01440
X01570Y01440
X00730Y01830
X01530Y01830
X01550Y02780
X01040Y02710
X01070Y01530
X01630Y01740
X00960Y01740
X00920Y00400
X04070Y04330
X00990Y00380
X01640Y02710
X00940Y02680
X01780Y02750
X01760Y01470
X00830Y01470
X04360Y03550
X01230Y02760
X01030Y01560
X04390Y04080
X01330Y01860
X01290Y00390
X04220Y05650
X03550Y05270
X03550Y04660
X03880Y05300
X03830Y04580
X02900Y04900
X02570Y04450
X04490Y04940
X04510Y04710
X02430Y04480
X02500Y04960
X02400Y04740
X03840Y04770
X03830Y04630
X02930Y05050
X02800Y05230
X02530Y05730
X04410Y05400
X02430Y05730
X04410Y05760
X01240Y01380
```

```
X01250Y03360
X00880Y00480
X02000Y01560
X01970Y02380
X00800Y02440
X00800Y02590
X00840Y02400
X00840Y01410
X01170Y01600
X02250Y04060
X02050Y03020
X01220Y03020
X01910Y05590
X00540Y04420
X01890Y04870
X01820Y05260
X01820Y02560
X01120Y02590
X01850Y04760
X01850Y02590
X01160Y03780
X04000Y05390
X02360Y02260
X01300Y02280
X03940Y03930
X02400Y03940
X04470Y05120
X04470Y03890
X02270Y02220
X01420Y02220
X02560Y05010
X02170Y02350
X02100Y04370
X01340Y04330
X03020Y02000
X01500Y02000
X01500Y01650
X02330Y03090
X00800Y02190
X02400Y02290
X01410Y00480
X01410Y00800
X01610Y01010
X03890Y02410
X02400Y03400
X02300Y03320
X04370Y03290
X02200Y03290
X04330Y03260
X02100Y03260
X04200Y03130
X02230Y02630
X04370Y03020
X02300Y03020
X02430Y02660
X02830Y04020
X04180Y02260
```

```
X02400Y02570
X02300Y02600
X02200Y02790
X03780Y02700
X02100Y02970
X00630Y02220
X00670Y02160
X01560Y02130
X02980Y03140
X00700Y03170
X01140Y00600
X01070Y02770
X00800Y03140
X03080Y03110
X03670Y03170
X01040Y01640
X01340Y01640
X03860Y03830
X03200Y03800
X01060Y02820
X01000Y03750
X00870Y00610
X03700Y03660
X03100Y03660
X01150Y02130
X03000Y03740
X01200Y03720
X00730Y02730
X00750Y00790
X02930Y03840
X03570Y03860
X00660Y02850
X00770Y00680
X02700Y03700
X02540Y02860
X04140Y02120
X04320Y05660
X04030Y05650
X04740Y05450
X02040Y05430
X00290Y05520
X04760Y05230
X03580Y05200
X04760Y04970
X04330Y04740
X04010Y04740
X03940Y04910
X02040Y04920
X00290Y04720
X02040Y04430
X03490Y04020
X02040Y03920
X00300Y03970
X02040Y03530
X03380Y03490
X02040Y03280
X00300Y03220
```

```
X04720Y02820
X03220Y02750
X02020Y02720
X04550Y02350
X00540Y02480
X04770Y01810
X01690Y01850
X00350Y01930
X02900Y01220
X00340Y01320
X04770Y04730
X04370Y05350
X04420Y04830
X03560Y04820
X04420Y05330
X04170Y05390
X04780Y04530
X03240Y04200
X00290Y04280
X02670Y02160
X00440Y02140
X04760Y01260
X04420Y01230
M00
X03250Y05100
X03250Y05600
X03370Y05100
X03370Y05600
X03070Y01900
X03270Y01900
X03700Y05500
X03700Y05600
M00
X00950Y00550
R31X00100
X00950Y00450
R31X00100
X00950Y00350
R31X00100
M00
X03500Y05100
M00
X03500Y05600
M00
X00500Y00625
X00500Y00275
X04500Y00275
X04500Y00625
M00
X00728Y00450
X04272Y00450
M00
X00500Y00450
X04500Y00450
M00
X00250Y00150
X00150Y02320
```

```
X00250Y05850
X02450Y05850
X04700Y05850
X04850Y02340
X04750Y00150
M30
```

B. NCROUTE FILE

```
;EXTENTS: -1.000  -1.000  10.000  7.500
;LEADER: 12
;HEADER: none
;CODE  : ASCII
;FILE  : brd23 for board
/tmp_mnt/h/galaxy_u1/mooney/thesis/project/brd23.brd
%
G90
F1
M16
T01
M16
G00X05000Y06000
M15
G01X05000Y00190
G01X04810Y00000
G01X00190Y00000
G01X00000Y00190
G01X00000Y06000
G01X05000Y06000
M16
G40
M30
```

APPENDIX C. DATASHEETS

The following Pages include manufacturer datasheets from the following companies:

- ***UTMC***
- ***Harris***
- ***Vitesse***
- ***IDT***
- ***National Semiconductor***
- ***ELCO***
- ***Phillips***
- ***Ralton***
- ***Ohmite***
- ***Motorola***

Military Standard Products

UT69RH051 MicroController

Product Brief

**UNITED
TECHNOLOGIES
MICROELECTRONICS
CENTER**

March 1995

FEATURES

☐ Three 16-bit timer/counters
  - High speed output
  - Compare/capture
  - Pulse width modulator
  - Watchdog timer capabilities

☐ 256 bytes of on-chip data RAM

☐ 32 programmable I/O lines

☐ 7 interrupt sources

☐ Programmable serial channel with:
  - Framing error detection
  - Automatic address recognition

☐ TTL and CMOS compatible logic levels

☐ 64K external data and program memory space

☐ MCS®-51 fully compatible instruction set

☐ Flexible clock operation
  - 1Hz to 20MHz with external clock
  - 2MHz to 20MHz using internal oscillator with external crystal

☐ Radiation-hardened process and design; total dose irradiation testing MIL-STD-883 Method 1019
  - Total dose: 1.0E6 rads(Si)
  - Single event upset: <25.6E-6 errors/device-day
  - Latchup immune

☐ Post-radiation AC/DC performance characteristics guaranteed to MIL-STD-883 Method 1019 testing at 1.0E6 rads (Si)

☐ Built on low-power, 1.2μ CMOS process

☐ Packaging options:
  - 40-pin DIP
  - 44-lead flatpack

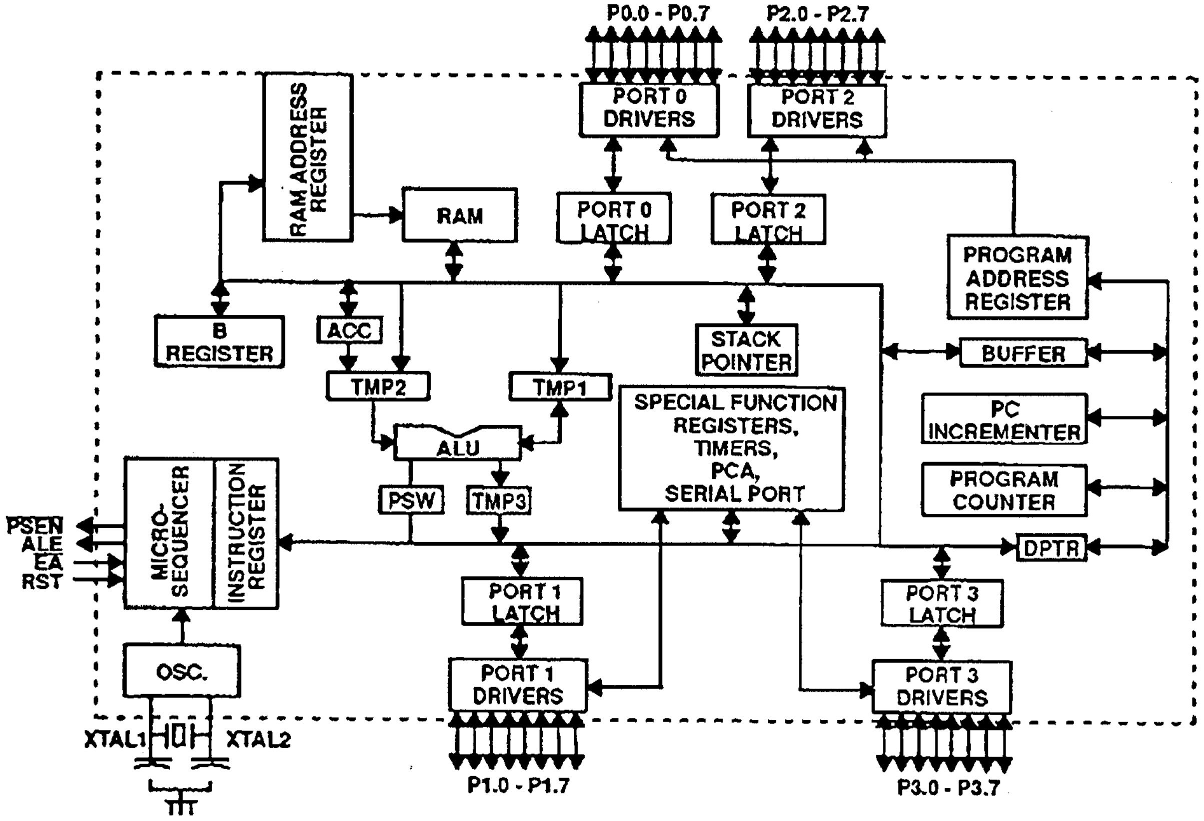


Figure 1. UT69RH051 MicroController Block Diagram

1.0 INTRODUCTION

The UT69RH051 is a radiation-tolerant 8-bit microcontroller that is pin equivalent to the Intel 8XC51FC microcontroller. The UT69RH051's static design allows operation from 1Hz to 20MHz. This product brief will describe hardware and software interfaces to the UT69RH051.

2.0 SIGNAL DESCRIPTION

V_{DD}: +5V Supply voltage

V_{SS}: Circuit Ground

Port 0 (P0.0 - P0.7): Port 0 is an 8-bit port. Its pins are used as the low-order multiplexed address and data bus during accesses to external program and data memory. Port 0 pins use strong internal pullups when emitting 1's, and are TTL compatible.

Port 1 (P1.0 - P1.7): Port 1 is an 8-bit bidirectional I/O port with internal pullups. The output buffers can drive TTL loads. When the Port 1 pins have 1's written to them, they are pulled high by the internal pullups and can be used as inputs in this state. As inputs, any pins that are externally pulled low will source current because of the pullups. In addition, Port 1 pins have the alternate uses shown in table 1.

Port 2 (P2.0 - P2.7): Port 2 is an 8-bit port. Its pins are used as the high-order address bus during accesses to external Program Memory and during accesses to external Data Memory that uses 16-bit addresses (i.e., MOVX@DPTR). It uses strong internal pullups when emitting 1's in this mode. During operations that do not require a 16-bit address, Port 2 emits the contents of the P2 Special Function Registers (SFR). The pins have internal pullups and can drive TTL loads.

Port 3 (p3.0 - p3.7): Port3 is an 8-bit bidirectional I/O port with internal pullups. The output buffers can drive TTL loads. When the Port 3 pins have 1's written to them, they are pulled high by the internal pullups and can be used as inputs in this state. As inputs, any pins that are externally pulled low will source current because of the pullups. In addition, Port 3 pins have the alternate uses shown in table 2.

Table 1. Port 1 Alternate Functions

Port Pin	Alternate Name	Alternate Function
P1.0	T2	External clock input to Timer/ Counter 2
P1.1	T2EX	Timer/Counter 2 Capture/Reload trigger and direction control
P1.2	ECI	External count input to PCA
P1.3	CEX0	External I/O for PCA capture/ compare Module 0
P1.4	CEX1	External I/O for PCA capture/ compare Module 1
P1.5	CEX2	External I/O for PCA capture/ compare Module 2
P1.6	CEX3	External I/O for PCA capture/ compare Module 3
P1.7	CEX4	External I/O for PCA capture/ compare Module 4

Table 2. Port 3 Alternate Functions

Port Pin	Alternate Name	Alternate Function
P3.0	RXD	Serial port input
P3.1	TXD	Serial port output
P3.2	$\overline{\text{INT0}}$	External interrupt 0
P3.3	$\overline{\text{INT1}}$	External interrupt 1
P3.4	T0	External clock input for Timer 0
P3.5	T1	External clock input for Timer 1
P3.6	$\overline{\text{WR}}$	External Data Memory write strobe
P3.7	$\overline{\text{RD}}$	External Data Memory read strobe

RST: Reset Input. A high on this input for one oscillator period while the oscillator is running resets the device. All ports and SFRs reset to their default conditions. Internal data memory is undefined after reset. Program execution begins within 12 oscillator periods (one machine cycle) after the RST signal is brought low. RST contains an internal pulldown resistor to allow implementing power-up reset with only an external capacitor.

ALE: Address Latch Enable. The ALE output is a pulse for latching the low byte of the address during accesses to external memory. In normal operation the ALE pulse is output every sixth oscillator cycle and may be used for external timing or clocking. However, during each access to external Data Memory (MOVX instruction), one ALE pulse is skipped.

$\overline{\text{PSEN}}$: Program Store Enable. This active low signal is the read strobe to the external program memory. $\overline{\text{PSEN}}$ is activated every sixth oscillator cycle except that two $\overline{\text{PSEN}}$ activations are skipped during external data memory accesses.

$\overline{\text{EA}}$: External Access Enable. This pin should be strapped to V_{SS} (Ground) for the UT69RH051.

XTAL1: Input to the inverting oscillator amplifier.

XTAL2: Output from the inverting oscillator amplifier.

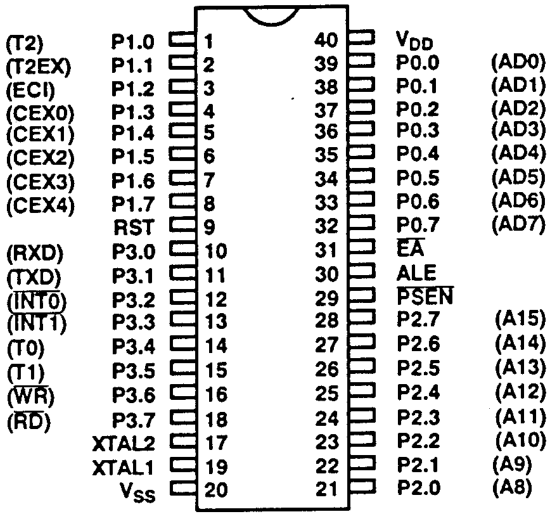


Figure 2. UT69RH051 Pin Connections

2.1 Hardware/Software Interface

2.1.1 Memory

The UT69RH051 has a separate address space for Program and Data Memory. Internally the UT69RH051 contains 256 bytes of Data Memory. It can address up to 64Kbytes of external Data Memory and 64Kbytes of external Program Memory.

2.1.1.1 Program Memory

There is no internal program memory in the UT69RH051. All program memory is accessed as external through ports P0 and P2. The $\overline{\text{EA}}$ pin must be tied to V_{SS} (ground) to enable access to external locations 0000_H through $7FFF_H$.

2.1.1.2 Data Memory

The UT69RH051 implements 256 bytes of internal data RAM. The upper 128 bytes of this RAM occupy a parallel address space to the SFRs. The CPU determines if the internal access to an address above 7FH is to the upper 128 bytes of RAM or to the SFR space by the addressing mode of the instruction. If direct addressing is used, the access is to the SFR space. If indirect addressing is used, the access is to the internal RAM. Stack operations are indirectly addressed so the upper portion of RAM can be used as stack space. Figure 3 shows the organization of the internal Data Memory.

The first 32 bytes are reserved for four register banks of eight bytes each. The processor uses one of the four banks as its working registers depending on the RS1 and RS0 bits in the PSW SFR. At reset, bank 0 is selected. If four register banks are not required, use the unused banks as general purpose scratch pad memory. The next 16 bytes (128 bits) are individually bit addressable. The remaining bytes are byte addressable and can be used as general purpose scratch pad memory. For addresses 0 - $7F_H$, use either direct or indirect addressing. For addresses larger than $7F_H$, use only indirect addressing.

In addition to the internal Data Memory, the processor can access 64 Kbytes of external Data Memory. The MOVX instruction accesses external Data Memory.

2.1.2 Special Function Registers

Table 3 contains the SFR memory map. Unoccupied addresses are not implemented on the device. Read accesses to these addresses will return unknown values and write accesses will have no effect.

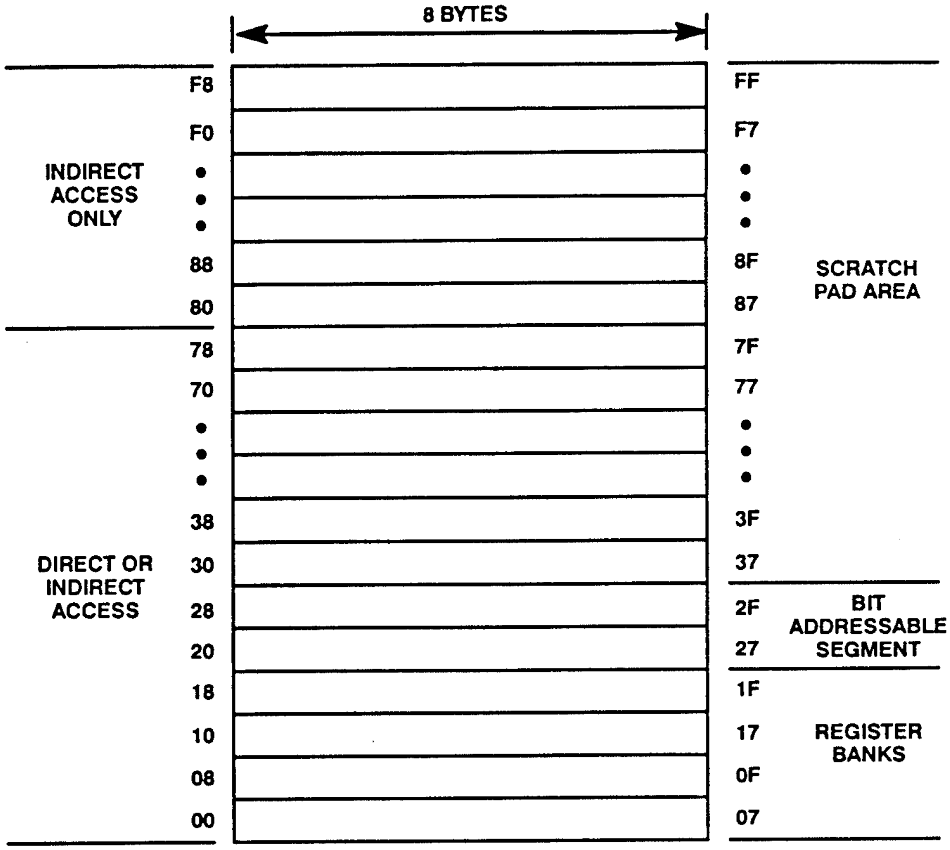


Figure 3. Internal Data Memory Organization

2.1.3 Reset

The reset input is the RST pin. To reset, hold a the RST pin high for a minimum of 24 oscillator period while the oscillator is running. The CPU generates an internal reset from the external signal. The ports pins are driven to the reset state as soon as a valid high is detected on the RST pin.

While RST is high, $\overline{\text{PSEN}}$, ALE, and the port pins are pulled weakly high. All SFRs are reset to their reset values as shown in table 3. The internal Data Memory content is indeterminate.

The processor will begin operation one machine cycle after the RST line is brought low. A memory access occurs immediately after the RST line is brought low, but the data is not brought into the processor. The memory access repeats on the next machine cycle and actual processing begins at that time.

2.1.4 Instruction Set

The instruction set for the UT69RH051 is compatible to the Intel MCS-51 instruction set used on the 8XC51FC.

Table 3. SFR Memory Registers

F8		CH 00000000	CCAP0H XXXXXXXX	CCAP1H XXXXXXXX	CCAP2H XXXXXXXX	CCAP3H XXXXXXXX	CCAP4H XXXXXXXX		FF
F0	B 00000000								F7
E8		CL 00000000	CCAP0L XXXXXXXX	CCAP1L XXXXXXXX	CCAP2L XXXXXXXX	CCAP3L XXXXXXXX	CCAP4L XXXXXXXX		EF
E0	ACC 00000000								E7
D8	CCON 00X00000	CMOD OOXXX000	CCAPM0 X00000000	CCAPM1 X00000000	CCAPM2 X00000000	CCAPM3 X00000000	CCAPM4 X00000000		DF
D0	PSW 00000000								D7
C8	T2CON 00000000	T2MOD XXXXXX00	RCAP2L 00000000	RCAP2H 00000000	TL2 00000000	TH2 00000000			CF
C0									C7
B8	IP X0000000	SADEN 00000000							BF
B0	P3 11111111							IPH X00000000	B7
A8	IE 00000000	SADDR 00000000							AF
A0	P2 11111111								A7
98	SCON 00000000	SBUF XXXXXXXX							9F
90	P1 11111111								97
88	TCON 00000000	TMOD 00000000	TL0 00000000	TL1 00000000	TH0 00000000	TH1 00000000			8F
80	P0 11111111	SP 00000111	DPL 00000000	DPH 00000000				PCON 00XX00XX	87

Notes:
1. Values shown are the reset values of the registers.
2. X = undefined.

3.0 RADIATION HARDNESS

The UT69RH051 incorporates special design and layout features which allow operation in high-level radiation environments. UTMC has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process. In addition, UTMC pays special attention to power and ground distribution during the design phase, minimizing dose-rate upset caused by rail collapse.

RADIATION HARDNESS DESIGN SPECIFICATIONS [1]

PARAMETER	CONDITION	MINIMUM	UNIT
Total Dose	+25°C per MIL-STD-883 Method 1019	1.0E6	rads(Si)
Dose Rate Upset	≤ 4µs pulsewidth	1.0E8	rads(Si)/sec
Dose Rate Survival	20ns pulsewidth	1.0E10	rads(Si)/sec
LET Threshold	-55°C to +125°C	36	MeV-cm^2/mg
Neutron Fluence	1MeV equivalent	1.0E14	n/cm^2

Note:
1. The UT69RH051 will not latchup during radiation exposure under recommended operating conditions.

4.0 ABSOLUTE MAXIMUM RATINGS [1]
(Referenced to V_{SS})

SYMBOL	PARAMETER	LIMITS	UNITS
V_{DD}	DC Supply Voltage	-0.5 to 7.0	V
$V_{I/O}$	Voltage on Any Pin	-0.5 to V_{DD}+3V	V
T_{STG}	Storage Temperature	-65 to +150	°C
P_D	Maximum Power Dissipation	750	mW
T_J	Maximum Junction Temperature	175	°C
Θ_{JC}	Thermal Resistance, Junction-to-Case [2]	10	°C/W
I_I	DC Input Current	± 10	mA

Notes:
1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Test per MIL-STD-883, Method 1012.

6.0 DC ELECTRICAL CHARACTERISTICS (Pre/Post-Radiation)*

V_{DD} = 5.0V ± 10%; TA = -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level Input Voltage		-0.5	.8	V
V_{IH}	High-level Input Voltage (except XTAL2, RST, $\overline{EA}$)		2.0	V_{DD}+0.3	V
V_{IH1}	High-level Input Voltage (XTAL, RST)		3.85	V_{DD}+0.3	V
V_{OL}	Low-level Output Voltage[1] (Ports 1, 2 and 3)	I_{OL} = 100µA		0.3	V
		I_{OL} = 1.6mA		0.45	V
		I_{OL} = 3.5mA		1.0	V
V_{OL1}	Low-level Output Voltage[1] (Port 0, ALE/$\overline{PROG}$, $\overline{PSEN}$)	I_{OL} = 200µA		0.3	V
		I_{OL} = 3.2mA		0.45	V
		I_{OL} = 7.0mA		1.0	V
V_{OH}	High-level Output Voltage (Ports 1, 2, and 3 ALE/$\overline{PROG}$ and $\overline{PSEN}$)	I_{OH} = -10µA	4.2		V
		I_{OH} = -30µA	3.8		V
		I_{OH} = -60µA	3.0		V
V_{OH1}	High-level Output Voltage (Port 0 in External Bus Mode)	I_{OH} = -200µA	4.2		V
		I_{OH} = -3.2mA	3.8		V
		I_{OH} = -7.0mA	3.0		V
I_{IL}	Logical 0 Input Current (Ports 1, 2, and 3)	V_{IN} = 0.45V		-50	µA
I_{LI}	Input Leakage Current (Port 0)	V_{IN} = V_{IL} or V_{IH}		± 10	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, and 3)	V_{IN} = 2V		-650	µA
C_{IO}	Pin Capacitance	@ 1MHZ, 25°C		10	pF
I_{CC}	Power Supply Current: (Running at 16MHz)	Note 2		52	mA

Notes:

* Post-radiation performance guaranteed at 25°C per MIL-STD-883.

1. Under steady state (non-transient) conditions, I_{OL} must be limited externally as follows:
   Maximum I_{OL} per port pin: 10mA
   Maximum I_{OL} per 8-bit port-
   Port 0: 26mA
   Ports 1, 2, & 3: 15mA
   Maximum total I_{OL} for all output pins: 71mA

   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. See figures 4, 5, and 6 for test conditions.

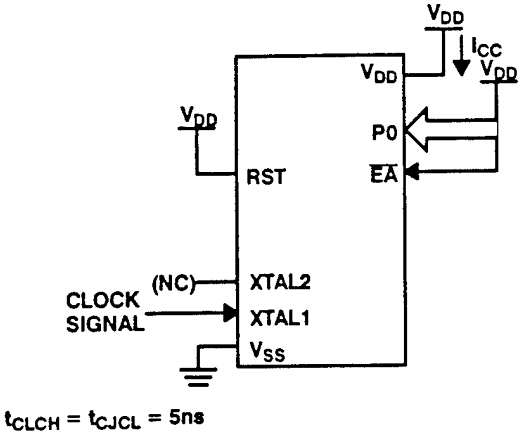


Figure 4. I_{DD} Test Condition, Active Mode
All other pins disconnected

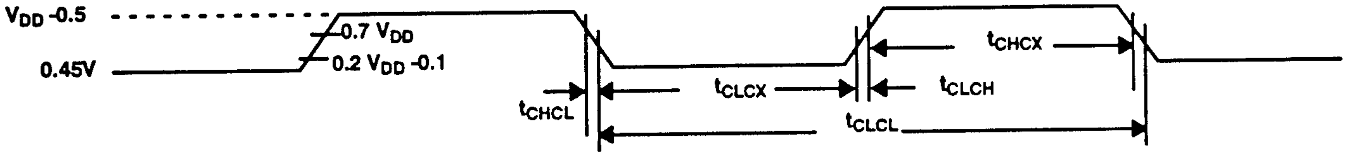


Figure 5. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes
$t_{CLCH} = t_{CHCL} = 5ns$

7.0 AC CHARACTERISTICS READ CYCLE (Post-Radiation)*

(V_{DD} = 5.0V ± 10%; -55°C < T_C < +125°C)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{CLCL}	Clock Period	50		ns
$1/t_{CLCL}$	Oscillator Frequency		16	MHz
t_{LHLL}	ALE Pulse Width	2 t_{CLCL}-40		ns
t_{AVLL}	Address Valid to ALE Low	t_{CLCL}-40		ns
t_{LLAX}	Address Hold after ALE Low	t_{CLCL}-30		ns
t_{LLIV}	ALE Low to Valid Instruction In		4 t_{CLCL}-100	ns
t_{LLPL}	ALE Low to $\overline{\text{PSEN}}$ Low	t_{CLCL}-30		ns
t_{PLPH}	$\overline{\text{PSEN}}$ Pulse Width	3 t_{CLCL}-45		ns
t_{PLIV}	$\overline{\text{PSEN}}$ Low to Valid Instruction In		3 t_{CLCL}-105	ns
t_{PXIX}	Input Instruction Hold after $\overline{\text{PSEN}}$	0		ns
t_{PXIZ}	Input Instruction Float After $\overline{\text{PSEN}}$		t_{CLCL}-25	ns
t_{AVIV}	Address to Valid Instruction In		5 t_{CLCL}-105	ns
t_{PLAZ}	$\overline{\text{PSEN}}$ Low to Address Float		10	ns
t_{RLRH}	$\overline{\text{RD}}$ Pulse Width	6 t_{CLCL}-100		ns
t_{WLWH}	$\overline{\text{WR}}$ Pulse Width	6 t_{CLCL}-100		ns
t_{RLDV}	$\overline{\text{RD}}$ Low to Valid Data In		5 t_{CLCL}-165	ns
t_{RHDX}	Data Hold After $\overline{\text{RD}}$	0		ns
t_{RHDZ}	Data Float After $\overline{\text{RD}}$		2 t_{CLCL}-60	ns
t_{LLDV}	ALE Low Valid Data In		8 t_{CLCL}-150	ns
t_{AVDV}	Address to Valid Data In		9 t_{CLCL}-165	ns
t_{LLWL}	ALE Low to $\overline{\text{RD}}$ or $\overline{\text{WR}}$ Low	3 t_{CLCL}-50	3 t_{CLCL}+50	ns
t_{AVWL}	Address Valid to $\overline{\text{WR}}$ Low	4 t_{CLCL}-130		ns
t_{QVWX}	Data Valid Before $\overline{\text{WR}}$	t_{CLCL}-50		ns
t_{WHQX}	Data Hold After $\overline{\text{WR}}$	t_{CLCL}-50		ns
t_{QVWH}	Data Valid to $\overline{\text{WR}}$ High	7 t_{CLCL}-150		ns
t_{RLAZ}	$\overline{\text{RD}}$ Low to Address Float		0	ns
t_{WHLH}	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE High	t_{CLCL}-40	t_{CLCL}+40	ns

Note:
- * Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).

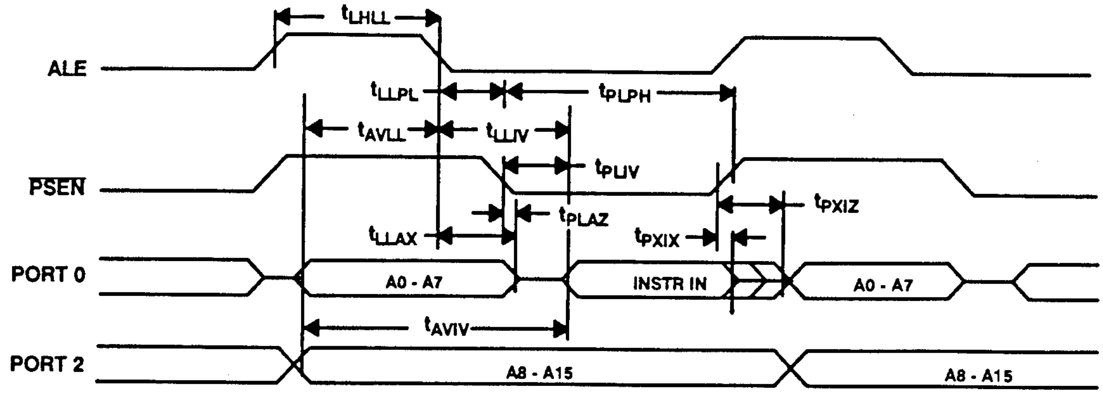


Figure 6. External Program Memory Read Timing Waveforms

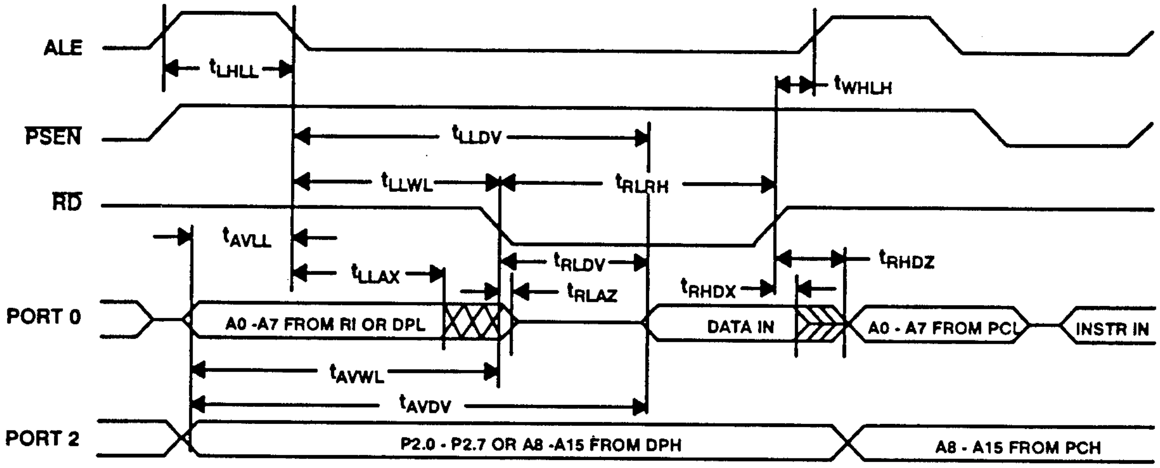


Figure 7. External Data Memory Read Cycle Waveforms

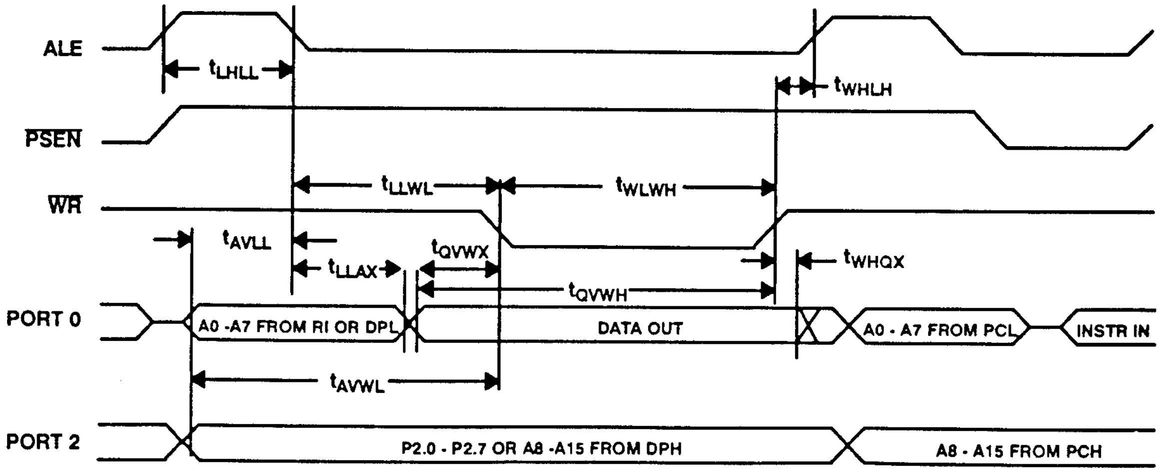


Figure 8. External Data Memory Write Cycle Waveforms

8.0 SERIAL PORT TIMING CHARACTERISTICS

($V_{DD} = 5.0V \pm 10\%$; $-55°C < T_C < +125°C$)

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{XLXL}	Serial Port Clock Period	12 t_{CLCL}-10	12 t_{CLCL}+10	ns
t_{QVXH}	Output Data Setup to Clock Rising Edge	10 t_{CLCL}-133		ns
t_{XHQX}	Output Data Hold after Clock Rising Edge	2 t_{CLCL}-70		ns
t_{XHDX}	Input Data Hold after Clock Rising Edge	0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		10 t_{CLCL}-133	ns

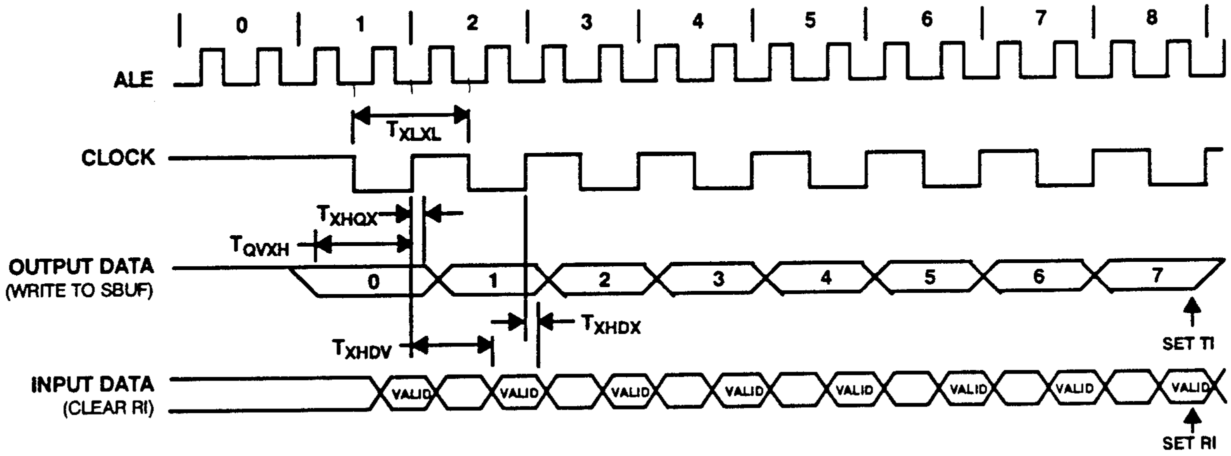


Figure 9. Serial Port Timing Waveforms

9.0 EXTERNAL CLOCK DRIVE TIMING CHARACTERISTICS

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
$1/t_{CLCL}$	Oscillator Frequency		16	MHz
t_{CHCX}	High Time	20		ns
t_{CLCX}	Low Time	20		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

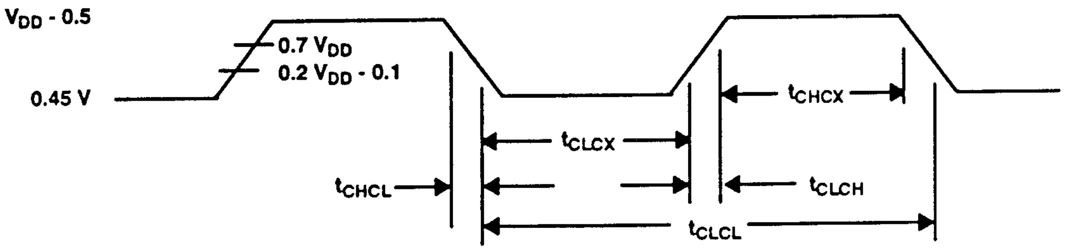
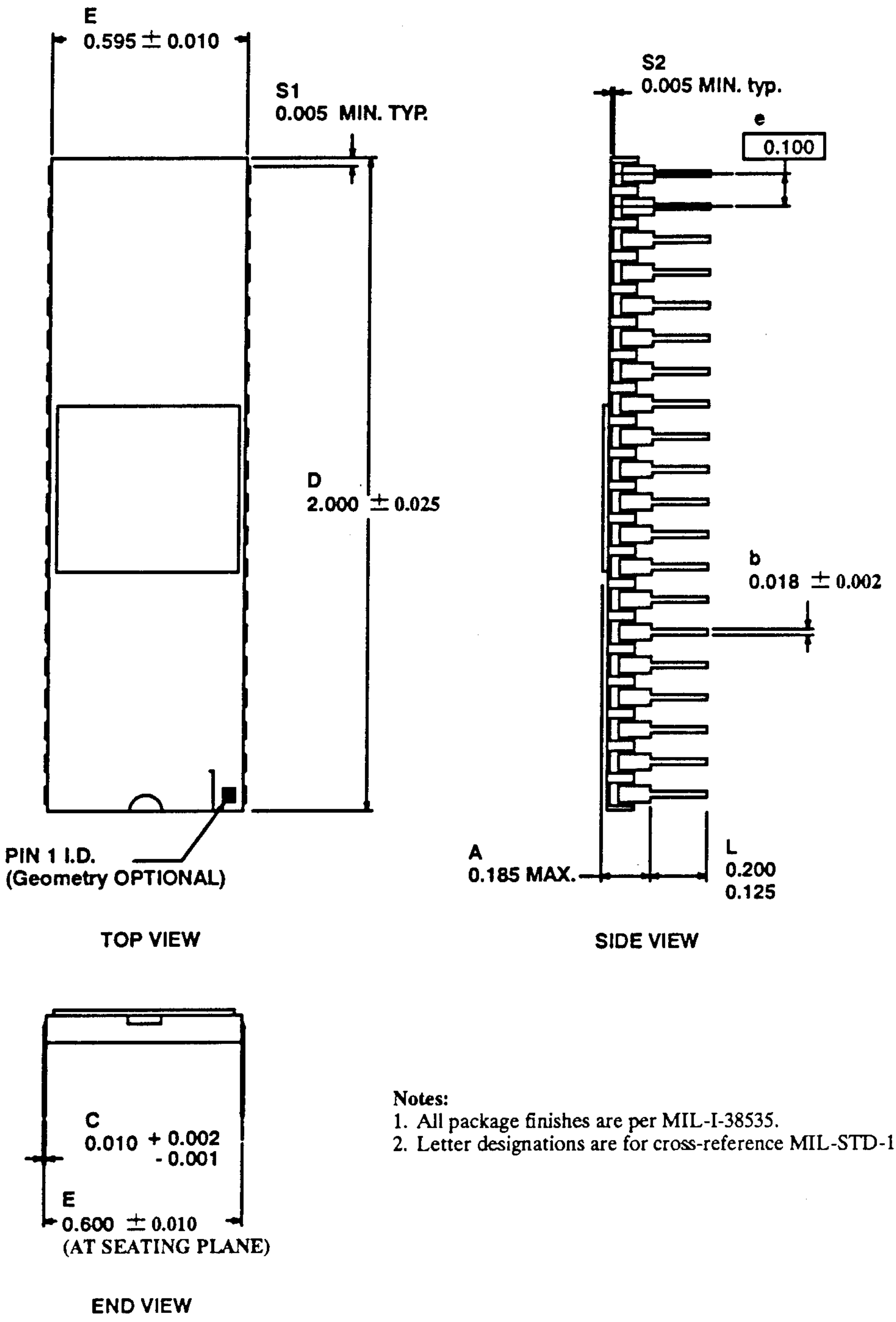


Figure 10. External Clock Drive Timing Waveforms

TBD

Figure 12. 44-Lead Flatpack

10.0 PACKAGING



Notes:
1. All package finishes are per MIL-I-38535.
2. Letter designations are for cross-reference MIL-STD-1835.

Figure 11. 40-pin Side-Brazed DIP

APPENDIX A
Difference Between Intel 8XC51FC and UTMC69RH051

There are a few areas in which the UT69RH051 differs from the 8XC51FC. These differences will be covered in this section. In this discussion, 8XC51FC will be used generically to refer to all speed grades of the Intel 8XC51FC family, including the 20MHz 8XC51FC-1.

1.0 RESET

The UT69RH051 requires the RST input to be held high for at least 24 oscillator periods to guarantee the reset is completed in the chip. Also, the port pins are reset asynchronously as soon as the RST pin is pulled high. On the UT69RH051 all portions of the chip are reset synchronously when the RST pin is high during a rising edge of the input clock. When coming out of reset, the 8XC51FC takes 1 to 2 machine cycles to begin driving ALE and $\overline{\text{PSEN}}$ immediately after the RST is removed but the access during the first machine cycle after reset is ignored by the processor. The second cycle will repeat the access and processing will begin.

2.0 POWER SAVING MODES OF OPERATION

2.1 Idle Mode

Idle mode and the corresponding control bit in the PCON SFR have not been implemented in the UT69RH051. Setting the idle control bit will have no effect.

2.2 Power Down Mode

Power down mode and the corresponding control bit in the PCON register have not been implemented in the UT69RH051. Setting the power down control bit will have no effect. Also, the Power Off Flag in the PCON has not been implemented.

3.0 ON CIRCUIT EMULATION

The On Circuit Emulation mode of operation in the 8XC51FC has not been implemented in the UT69RH051.

4.0 OPERATING CONDITIONS

The operating voltage range for the 8XC51FC is 5V ± 20%. The operating temperature range is 0° to 70°C. On the UT69RH051, the operating voltage range is 5V ± 10%. The operating temperature range is -55° to +125°C.

APPENDIX B
Impact of External Program ROM

The 8051 family of microcontrollers, including the 8XC51FC, use ports 0 and 2 to access external memory. In implementations with external program memory, these two ports are dedicated to the program ROM interface and can not be used as Input/Output ports. The UT69RH051 uses external program ROM, so ports 0 and 2 will not be available for I/O.

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Columbia, MD 21046
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Boston Sales Office
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Braintree, MA 02184
617-356-5600

North LA Sales Office
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Camarillo, CA 93010
805-445-6665

UNITED TECHNOLOGIES MICROELECTRONICS CENTER

UT69RH051-1-3-95-PB

Military Standard Product

UT22VP10 Universal RADPAL™

Preliminary Data Sheet

UNITED TECHNOLOGIES MICROELECTRONICS CENTER

July 1995

FEATURES

☐ High speed Universal RADPAL
- t_{PD}: 25ns maximum
- f_{MAX1}: 30MHz maximum external frequency
- Supported by industry-standard programmer
- Amorphous silicon anti-fuse

☐ Asynchronous & synchronous RADPAL operation
- Synchronous PRESET
- Asynchronous RESET

☐ Up to 22 input and 10 output drivers may be configured
- CMOS & TTL-compatible input and output levels
- Three-state output drivers

☐ Variable product terms, 8 to 16 per output

☐ 10 user-programmable output macrocells
- Registered or combinatorial operation
- Output driver polarity control selectable
- 2 feedback paths available

☐ Low operating current
- I_{DD}: 60mA @ 1MHz

☐ V_{DD}: 5.0 volts ±10%

☐ Radiation-hardened process and design; total dose irradiation testing to MIL-STD-883, Method 1019
- Total dose: 1.0E6 rads(Si)
- Single event effects:
  Upset threshold 50 MeV-cm^2/mg (min)
  Latchup immune
- Neutron fluence: 1.0E14 n/cm^2

☐ QML Q & V compliant part (check factory for availability)

☐ Packaging options:
- 24-pin 100-mil center DIP (0.300 x 1.2)
- 24-lead flatpack (.45 x .64)
- 28-lead quad-flatpack (.45 x .45)

☐ Standard Military Drawing 5962-94754 available

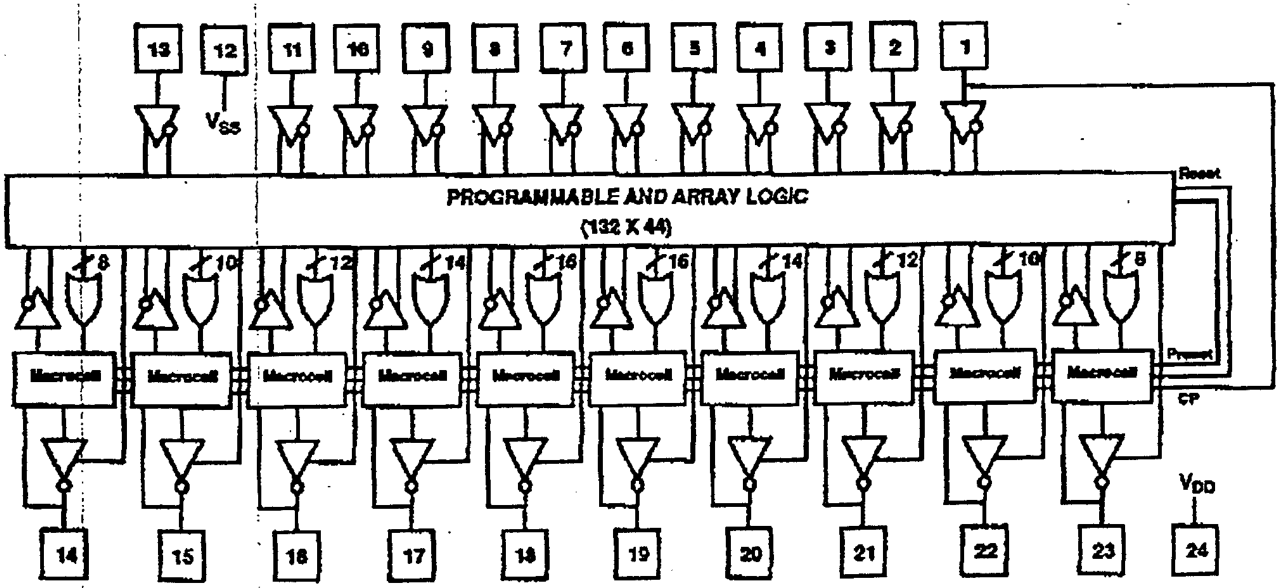


Figure 1. Block Diagram

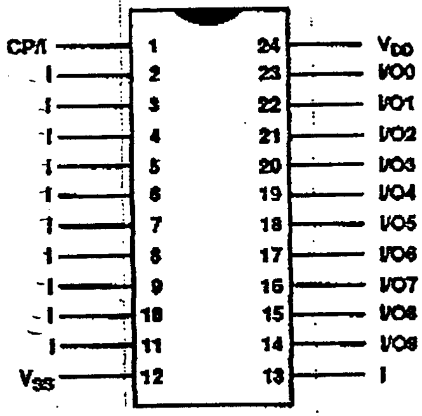
PRODUCT DESCRIPTION

The UT22VP10 RADPAL is a fuse programmable logic array device. The familiar sum-of-products (AND-OR) logic structure is complemented with a programmable macrocell. The UT22VP10 is available in 24-pin DIP, 24-lead flatpack, and 28-lead quad-flatpack package offerings providing up to 22 inputs and 10 outputs. Amorphous silicon anti-fuse technology provides the programming of each output. The user specifies whether each of the potential outputs is registered or combinatorial. Output polarity is also individually selected, allowing for greater flexibility for output configuration. A unique output enable function allows the user to configure bidirectional I/O on an individual basis.

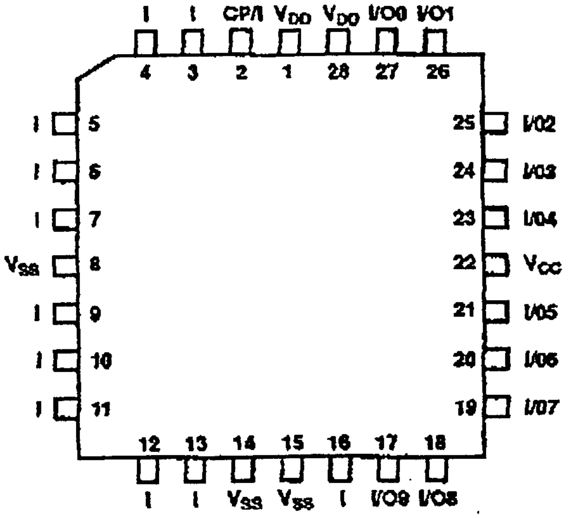
The UT22VP10 architecture implements variable product terms providing 8 to 16 product terms to outputs. This feature provides the user with increased logic function flexibility. Other features include common synchronous preset and asynchronous reset. These features eliminate the need for performing the initialization function.

The UT22VP10 provides a device with the flexibility to implement logic functions in the 500 to 800 gate complexity. The flexible architecture supports the implementation of logic functions requiring up to 21 inputs and only a single output or down to 12 inputs and 10 outputs.

DIP & FLATPACK PIN CONFIGURATION



QUAD-FLATPACK PIN CONFIGURATION



PIN NAMES

CP/I	Clock/Data Input
I	Data Input
I/O	Data Input/Output
V_{DD}	Power
V_{SS}	Ground

FUNCTION DESCRIPTION

The UT22VP10 RADPAL implements logic functions as sum-of-products expressions in a one-time programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Table 1. Macrocell Configuration Table

C_2	C_1	C_0	Output Type	Polarity	Feedback
0	0	0	Registered	Active LOW	Registered
0	0	1	Registered	Active HIGH	Registered
X	1	0	Combinatorial	Active LOW	I/O
X	1	1	Combinatorial	Active HIGH	I/O
1	0	0	Registered	Active LOW	I/O
1	0	1	Registered	Active HIGH	I/O

OVERVIEW

The UT22VP10 RADPAL architecture (figure 1) has 12 dedicated inputs and 10 I/Os to provide up to 22 inputs and 10 outputs for creating logic functions. At the core of the device is a one-time programmable anti-fuse AND array that drives a fixed OR array. With this structure, the UT22VP10 can implement up to 10 sum-of-products logic expressions.

Associated with each of the 10 OR functions is a macrocell which is independently programmed to one of six different configurations. The one-time programmable macro cells allow each I/O to create sequential or combinatorial logic functions with either Active-High or Active-Low polarity.

LOGIC ARRAY

The one-time programmable AND array of the UT22VP10 RADPAL is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 input lines

- 24 input lines carry the true and complement of the signals applied to the input pins
- 20 lines carry the true and complement values of feedback or input signals from the 10 I/Os

132 product terms:

- 120 product terms (arranged in 2 groups of 8, 10, 12, 14, and 16) used to form logic sums
- 10 output enable terms (one for each I/O)
- 1 global synchronous preset term
- 1 global asynchronous reset term

At each input-line/product-term intersection there is an anti-fuse cell which determines whether or not there is a logical connection at that intersection. A product term which is connected to both the true and complement of an input signal will always be logical zero, and thus will not effect the OR function that it derives. When there are no connections on a product term, a Don't Care state exists and that term will always be a logical one.

PRODUCT TERMS

The UT22VP10 provides 120 product terms that drive the 10 OR functions. The 120 product terms connect to the outputs in groups of 8, 10, 12, 14, and 16 to from logical sums.

MACROCELL ARCHITECTURE

The output macrocell provides complete control over the architecture of each output. Configuring each output independently permits users to tailor the configuration of the UT22VP10 to meet design requirements.

Each I/O macrocell (see figure 2) consists of a D flip-flop and two signal-select multiplexers. Three configuration select bits controlling the multiplexers determine the configuration of each UT22VP10 macrocell. The configuration select bits determine output polarity, output type (registered or combinatorial) and input feedback type (registered or I/O). See figure 3 for equivalent circuits for the macrocell configurations.

OUTPUT FUNCTIONS

The signal from the OR array may be fed directly to the output pin (combinatorial function) or latched in the D flip-flop (registered function). The D flip-flop latches data on the rising edge of the clock. When the synchronous preset term is satisfied, the Q output of the D flip-flop output will be set logical one at the next rising edge of the clock input. Satisfying the asynchronous clear term sets Q logical zero, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

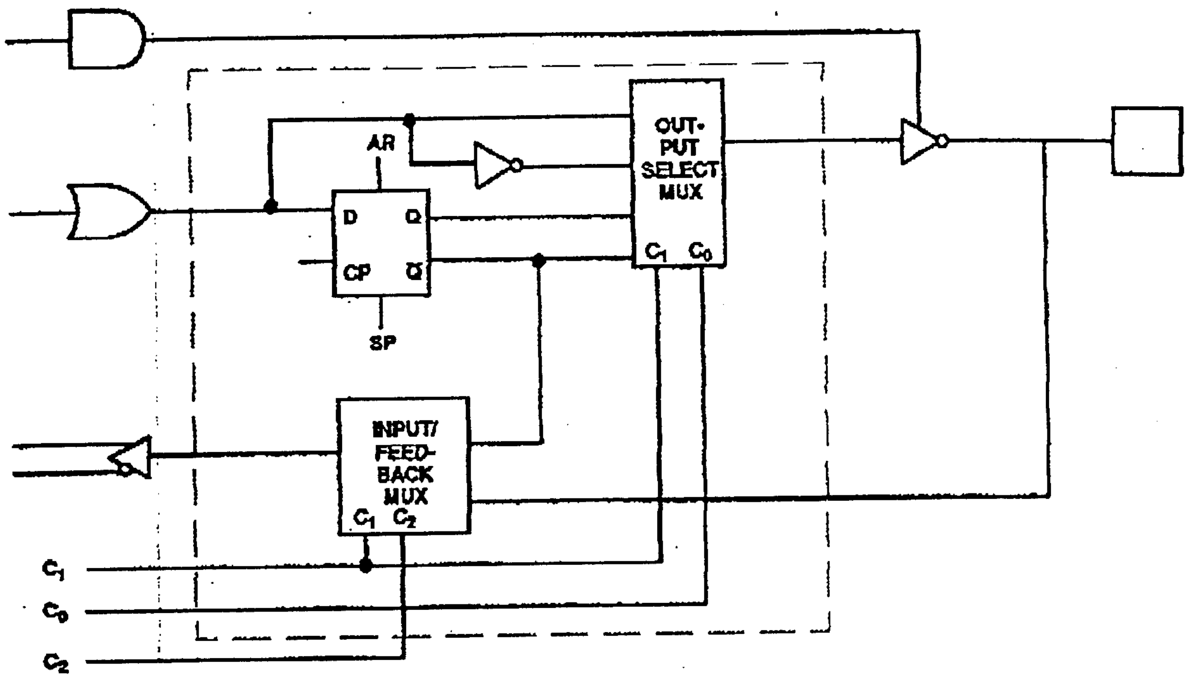


Figure 2. Macrocell

OUTPUT POLARITY

Each macrocell can be configured to implement Active-High or Active Low logic. Programmable polarity eliminates the need for external inverters. Unprogrammed device outputs are logical one (inputs don't care).

OUTPUT ENABLE

The output of each I/O macrocell can be enabled or disabled under the control a programmable output enable product term. The output signal is propagated to the I/O pin when the logical conditions programmed on the output enable term are satisfied. Otherwise, the output buffer is driven into the high-impedance state.

The output enable term allows the I/O pin to function as a dedicated input, dedicated output, or bidirectional I/O. When every connection is unprogrammed, the output enable product term permanently enables the output buffer and yields a dedicated output. If every connection is programmed, the enable term is logically low and the I/O functions as a dedicated input.

REGISTER FEEDBACK

The feedback signal to the AND array is taken from the $\overline{Q}$ output when the I/O macrocell implements a registered function ($C_2 = 0, C_1 = 0$).

BIDIRECTIONAL I/O

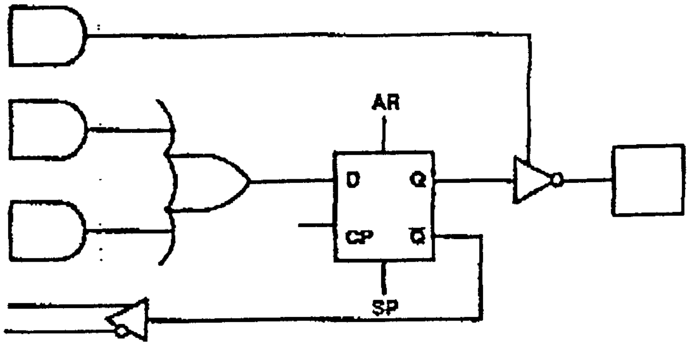
The feedback signal is taken from the I/O pin when the macrocell implements a combinatorial function ($C_1 = 1$) or a registered function ($C_2 = 1, C_1 = 0$). In this case, the pin can be used as a dedicated input, a dedicated output, or a bidirectional I/O.

POWER-ON RESET

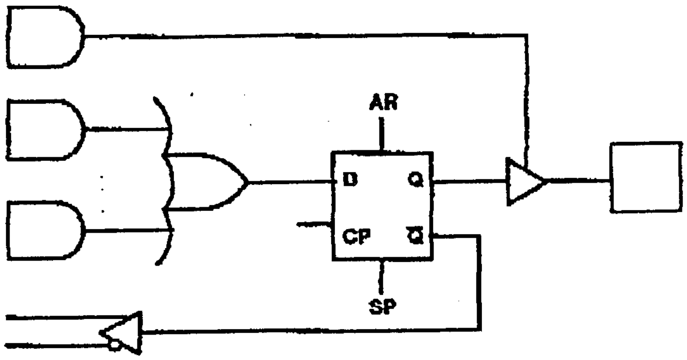
To ease system initialization, all D flip-flops will power-up to a reset condition and the Q output will be low. The actual output of the UT22VP10 will depend on the programmed output polarity. The V_{DD} rise must be monotonic and the reset delay time is 5μs maximum.

ANTI-FUSE SECURITY

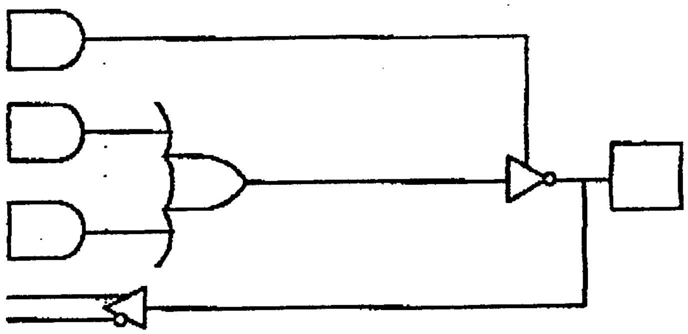
The UT22VP10 provides a special security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, at the conclusion of the programming cycle. Once the security bit is set it is impossible to verify (read) or program the UT22VP10.



Registered Feedback, Registered, Active-Low Output ($C_2 = 0, C_1 = 0, C_0 = 0$)

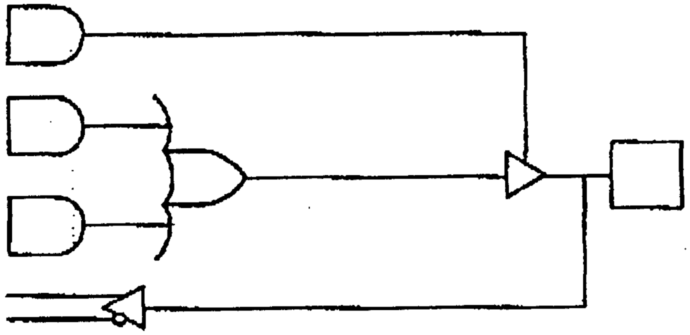


Registered Feedback, Registered, Active-High Output ($C_2 = 0, C_1 = 0, C_0 = 1$)

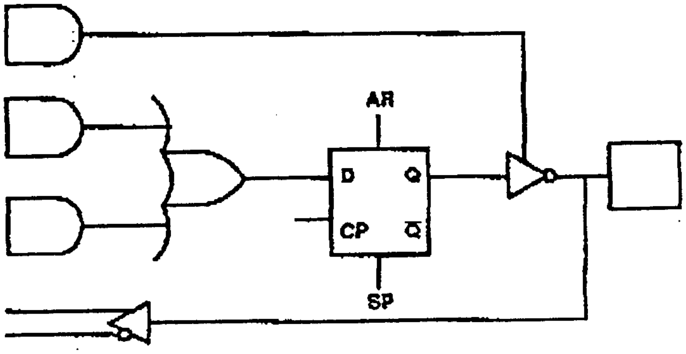


I/O Feedback, Combinatorial, Active-Low Output ($C_2 = X, C_1 = 1, C_0 = 0$)

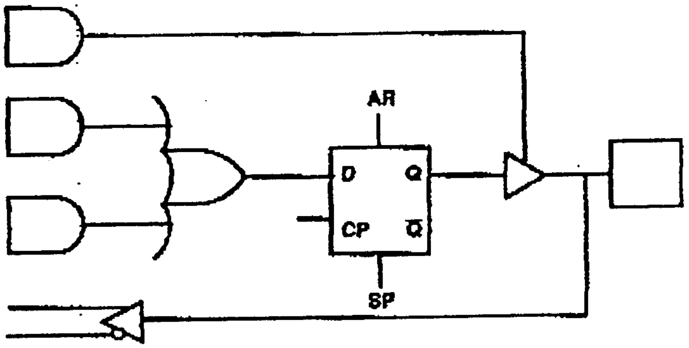
Figure 3. Macrocell Configuration *(continued on next page)*



I/O Feedback, Combinatorial, Active-High Output ($C_2 = X$, $C_1 = 1$, $C_0 = 1$)



I/O Feedback, Registered, Active-Low Output ($C_2 = 1$, $C_1 = 0$, $C_0 = 0$)



I/O Feedback, Registered, Active-High Output ($C_2 = 1$, $C_1 = 0$, $C_0 = 1$)

Figure 3. Macrocell Configuration

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	-0.3 to 7.0	V
$V_{I/O}$	Input voltage any pin	-0.3 to V_{DD} +.3	V
T_{STG}	Storage Temperature range	-65 to +150	°C
T_J	Maximum junction temperature	+175	°C
T_S	Lead temperature (soldering 5 seconds)	+300	°C
Θ_{JC}	Thermal resistance junction to case	20	°C/W
I_I	DC input current	±10	mA
P_D[2]	Maximum power dissipation	1.6	W

Notes:

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. (I_{CC} max + I_{OS}) 5.5V.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMIT	UNITS
V_{DD}	Supply voltage	4.5 to 5.5	V
V_{IN}	Input voltage any pin	0 to V_{DD}	V
T_C	Temperature range	-55 to + 125	°C

National Semiconductor

July 1992

100328
Low Power Octal ECL/TTL Bi-Directional Translator with Latch

General Description

The 100328 is an octal latched bi-directional translator designed to convert TTL logic levels to 100K ECL logic levels and vice versa. The direction of this translation is determined by the DIR input. A LOW on the output enable input (OE) holds the ECL outputs in a cut-off state and the TTL outputs at a high impedance level. A HIGH on the latch enable input (LE) latches the data at both inputs even though only one output is enabled at the time. A LOW on LE makes the 100328 transparent.

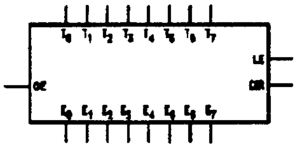
The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitter-followers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

The 100328 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have 50 kΩ pull-down resistors.

Features

- Identical performance to the 100128 at 50% of the supply current
- Bi-directional translation
- 2000V ESD protection
- Latched outputs
- FAST® TTL outputs
- TRI-STATE® outputs
- Voltage compensated operating range = −4.2V to −5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

Logic Symbol



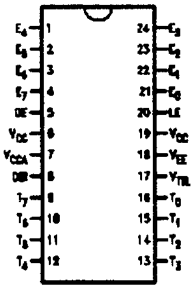
TL/F/10219–1

Pin Names	Description
E_0–E_7	ECL Data I/O
T_0–T_7	TTL Data I/O
OE	Output Enable Input
LE	Latch Enable Input
DIR	Direction Control Input

All pins function at 100K ECL levels except for T_0–T_7.

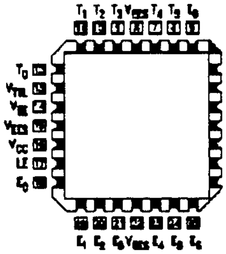
Connection Diagrams

24-Pin DIP/SOIC



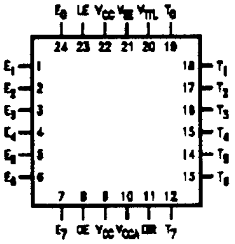
TL/F/10219–2

28-Pin PCC



TL/F/10219–3

24-Pin Quad Cerpak



TL/F/10219–4

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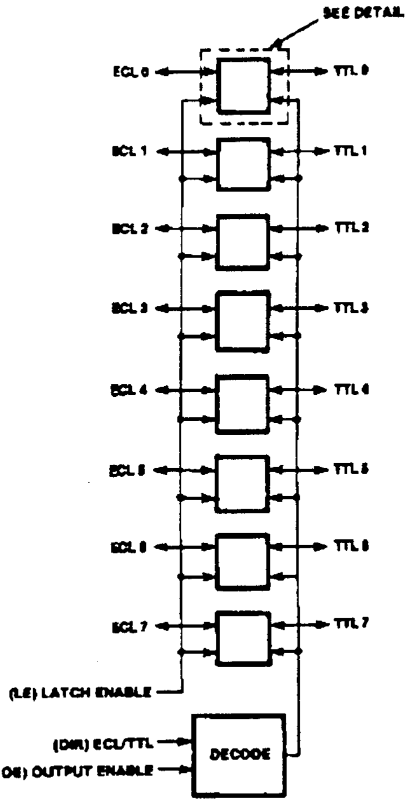
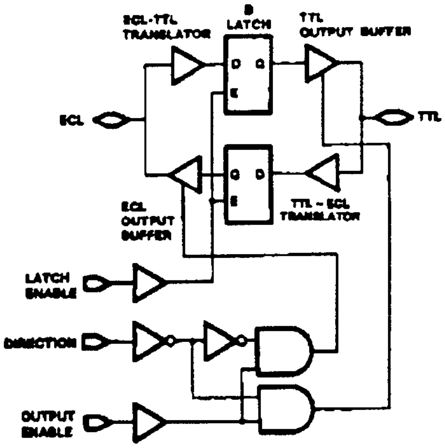
Functional Diagram



TL/F/10219-5

Note: LE, DIR, and OE use ECL logic levels

Detail



TL/F/10219-6

Truth Table

OE	DIR	LE	ECL Port	TTL Port	Notes
L	X	L	LOW (Cut-Off)	Z	
L	L	H	Input	Z	1, 3
L	H	H	LOW (Cut-Off)	Input	2, 3
H	L	L	L	L	1, 4
H	L	L	H	H	1, 4
H	L	H	X	Latched	1, 3
H	H	L	L	L	2, 4
H	H	L	H	H	2, 4
H	H	H	Latched	X	2, 3

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

Note 1: ECL input to TTL output mode.

Note 2: TTL input to ECL output mode.

Note 3: Retains data present before LE set HIGH.

Note 4: Latch is transparent.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	
Ceramic	+175°C
Plastic	+150°C
V_{EE} Pin Potential to Ground Pin	−7.0V to +0.5V
V_{TTL} Pin Potential to Ground Pin	−0.5V to +6.0V
ECL Input Voltage (DC)	V_{EE} to +0.5V
ECL Output Current (DC Output HIGH)	−50 mA
TTL Input Voltage (Note 3)	−0.5V to +6.0V
TTL Input Current (Note 3)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State TRI-STATE Output	−0.5V to +5.5V
Current Applied to TTL Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD (Note 2)	≥2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Note 3: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Case Temperature (T_C)	
Commercial	0°C to +85°C
Industrial	−40°C to +85°C
Military	−55°C to +125°C
ECL Supply Voltage (V_{EE})	−5.7V to −4.2V
TTL Supply Voltage (V_{TTL})	+4.5V to +5.5V

Commercial Version

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, V_{TTL} = +4.5V to +5.5V (Note 4)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	−1025	−955	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$ Loading with 50Ω to −2V
V_{OL}	Output LOW Voltage	−1830	−1705	−1620	mV	
	Cutoff Voltage		−2000	−1950	mV	OE or DIR Low, V_{IN} = $V_{IH(Max)}$ or V_{IL}(Min), Loading with 50Ω to −2V
V_{OHC}	Output HIGH Voltage Corner Point High	−1035			mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$ Loading with 50Ω to −2V
V_{OLC}	Output LOW Voltage Corner Point Low			−1610	mV	
V_{IH}	Input HIGH Voltage	2.0		5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0		0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current			70	μA	V_{IN} = +2.7V
	Breakdown Test			1.0	mA	V_{IN} = +5.5V
I_{IL}	Input LOW Current	−700			μA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2			V	I_{IN} = −18 mA
I_{EE}	V_{EE} Supply Current	−159 −169		−75 −75	mA	LE Low, OE and DIR High Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V

Note 4: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Commercial Version (Continued)

ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = 0°C to +85°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V (Note)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage	2.7 2.4	3.1 2.9		V V	I_{OH} = −3 mA, V_{TTL} = 4.75V I_{OH} = −3 mA, V_{TTL} = 4.50V
V_{OL}	Output LOW Voltage		0.3	0.5	V	I_{OL} = 24 mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	−1165		−870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	−1830		−1475	mV	Guaranteed LOW Signal for All Inputs
I_{IH}	Input HIGH Current			350	μA	V_{IN} = V_{IH} (Max)
I_{IL}	Input LOW Current	0.50			μA	V_{IN} = V_{IL} (Min)
I_{OZHT}	TRI-STATE Current Output High			70	μA	V_{OUT} = +2.7V
I_{OZLT}	TRI-STATE Current Output Low	−700			μA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	−150		−60	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current			74 49 67	mA mA mA	TTL Outputs LOW TTL Outputs HIGH TTL Outputs in TRI-STATE

DIP TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND (Note)

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	T_N to E_n (Transparent)	1.1	3.5	1.1	3.6	1.1	3.8	ns ns	*Figures 1 & 2*
t_{PLH} t_{PHL}	LE to E_n	1.7	3.6	1.7	3.7	1.9	3.9	ns ns	*Figures 1 & 2*
t_{PZH}	OE to E_n (Cutoff to High)	1.3	4.2	1.5	4.4	1.7	4.8	ns	*Figures 1 & 2*
t_{PHZ}	OE to E_n (High to Cutoff)	1.5	4.5	1.6	4.5	1.6	4.6	ns	*Figures 1 & 2*
t_{PHZ}	DIR to E_n (High to Cutoff)	1.6	4.3	1.6	4.3	1.7	4.5	ns	*Figures 1 & 2*
t_{set}	T_n to LE	1.1		1.1		1.1		ns	*Figures 1 & 2*
t_{hold}	T_n to LE	1.1		1.1		1.1		ns	*Figures 1 & 2*
t_{pw}(H)	Pulse Width LE	2.1		2.1		2.1		ns	*Figures 1 & 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	*Figures 1 & 2*

Note: The specified limits represent the "worst" case value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

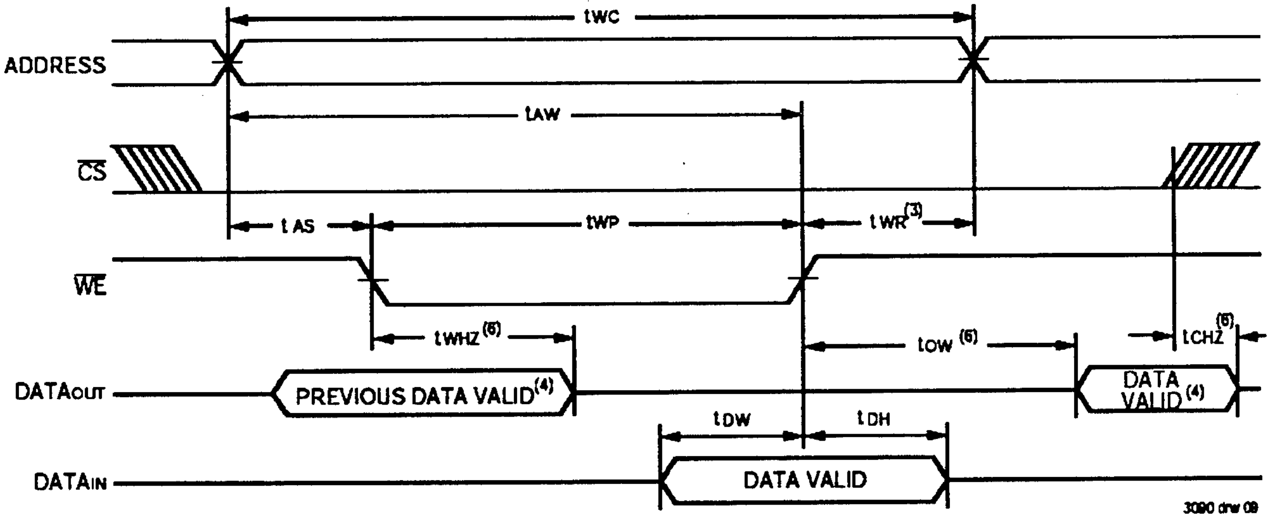
AC ELECTRICAL CHARACTERISTICS (CONTINUED) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA35 6168LA35		6168SA45(2) 6168LA45(2)		6168SA55(2) 6168LA55(2)		6168SA70(2) 6168LA70(2)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle										
t_{WC}	Write Cycle Time	30	—	40	—	50	—	60	—	ns
t_{CW}	Chip Select to End-of-Write	30	—	40	—	50	—	60	—	ns
t_{AW}	Address Valid to End-of-Write	30	—	40	—	50	—	60	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	30	—	40	—	50	—	60	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	15	—	20	—	20	—	25	—	ns
t_{DH}	Data Hold Time	0	—	3	—	3	—	3	—	ns
t_{WHZ}(3)	Write Enable to Output in High-Z	—	13	—	20	—	25	—	30	ns
t_{OW}(3)	Output Active from End-of-Write	0	—	0	—	0	—	0	—	ns

3090 tbl 15

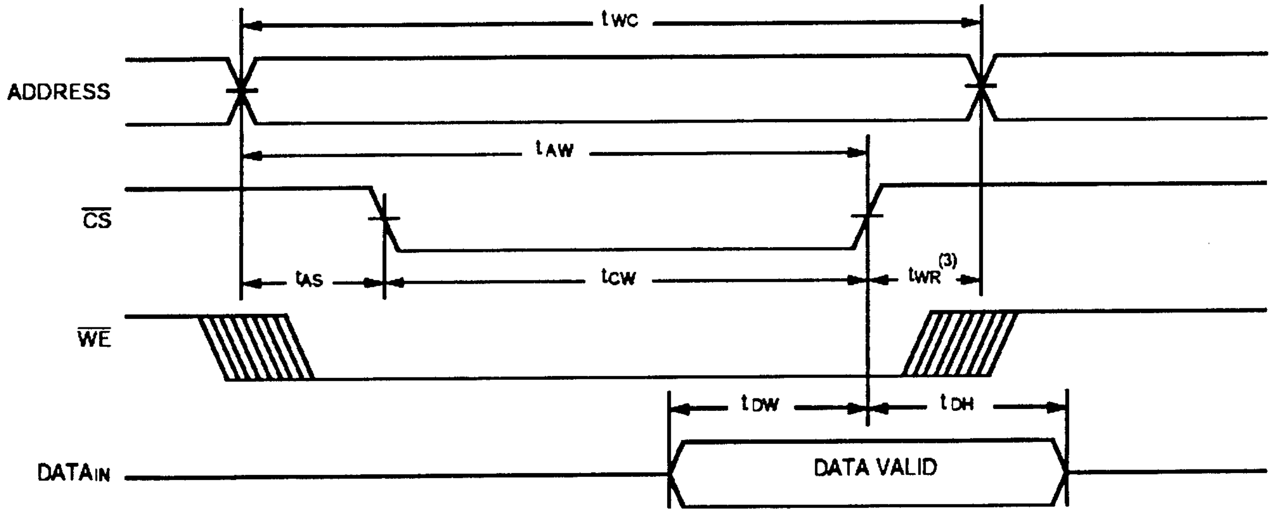
NOTES:
1. 0° to +70°C temperature range only.
2. –55°C to +125°C temperature range only. Also available 85ns and 100ns devices.
3. This parameter is guaranteed with the AC Load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 5)



3090 drw 09

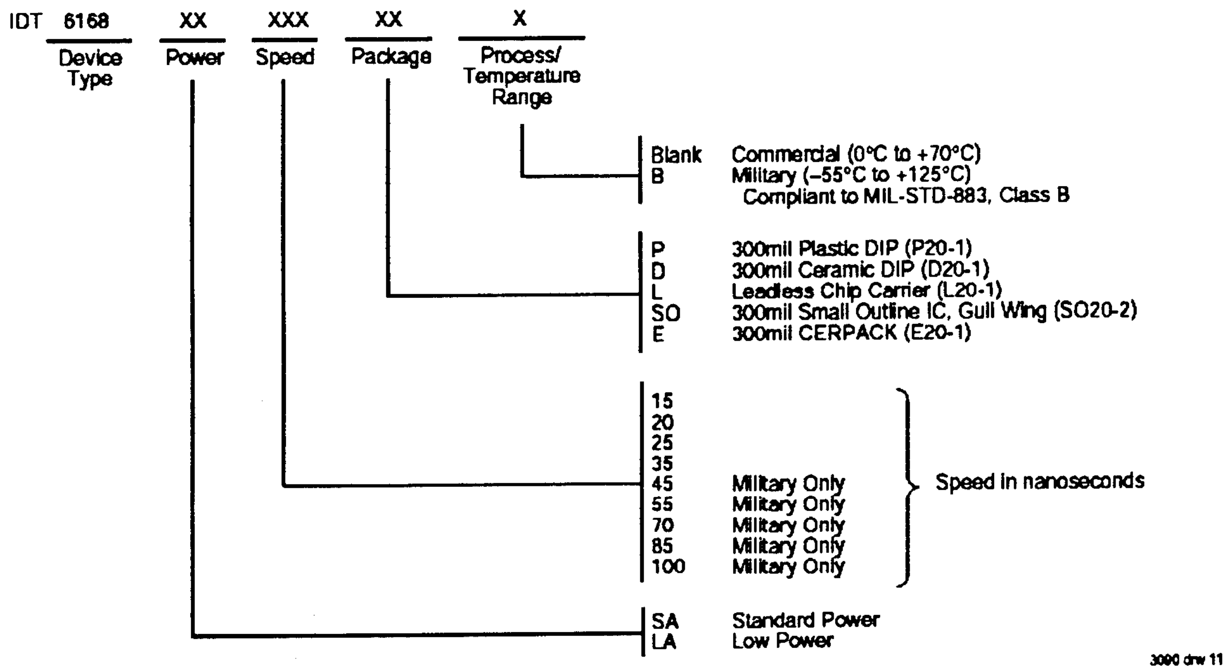
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS}}$ CONTROLLED TIMING)(1, 2, 5)



3080 drw 10

NOTES:
1. $\overline{\text{WE}}$ or $\overline{\text{CS}}$ must be HIGH during all address transitions.
2. A write occurs during the overlap of a LOW $\overline{\text{CS}}$ and a LOW $\overline{\text{WE}}$.
3. tWR is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going HIGH to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals should not be applied.
5. If the $\overline{\text{CS}}$ LOW transition occurs simultaneously with or after the $\overline{\text{WE}}$ LOW transition, the outputs remain in the high impedance state.
6. Transition is measured ±200mV from steady state.

ORDERING INFORMATION



Blank	Commercial (0°C to +70°C)
B	Military (–55°C to +125°C) Compliant to MIL-STD-883, Class B

P	300mil Plastic DIP (P20-1)
D	300mil Ceramic DIP (D20-1)
L	Leadless Chip Carrier (L20-1)
SO	300mil Small Outline IC, Gull Wing (SO20-2)
E	300mil CERPACK (E20-1)

15	
20	
25	
35	
45	Military Only
55	Military Only
70	Military Only
85	Military Only
100	Military Only

SA	Standard Power
LA	Low Power

3090 drw 11

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA15		6168SA20/25 6168LA20/25		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	15	—	20/25	—	ns
t_{AA}	Address Access Time	—	15	—	20/25	ns
t_{ACS}	Chip Select Access Time	—	15	—	20/25	ns
t_{CLZ}(2)	Chip Select to Output in Low-Z	3	—	5	—	ns
t_{CHZ}(2)	Chip Deselect to Output in High-Z	—	8	—	10	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	ns
t_{PU}(2)	Chip Select to Power-Up Time	0	—	0	—	ns
t_{PD}(2)	Chip Deselect to Power-Down Time	—	15	—	20/25	ns

3090 drw 12

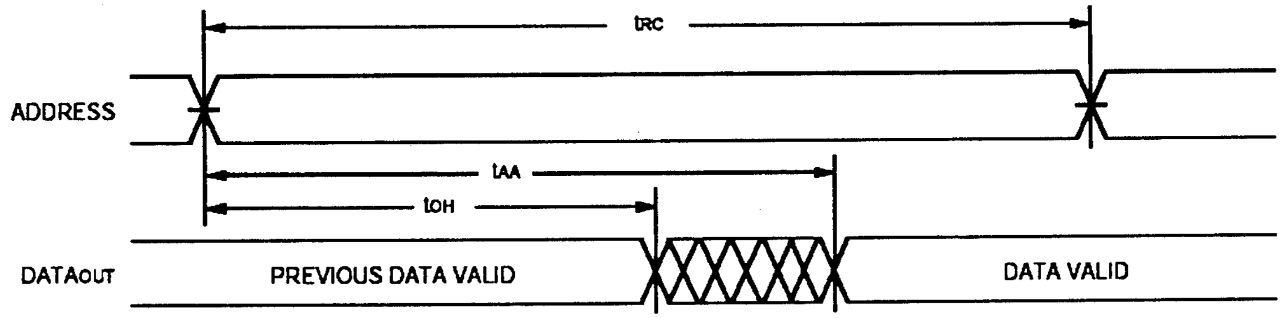
AC ELECTRICAL CHARACTERISTICS (CONTINUED) (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA35 6168LA35		6168SA45(1) 6168LA45(1)		6168SA55(1) 6168LA55(1)		6168SA70(1) 6168LA70(1)		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	35	—	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	—	70	ns
t_{ACS}	Chip Select Access Time	—	35	—	45	—	55	—	70	ns
t_{CLZ}(2)	Chip Select to Output in Low-Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}(2)	Chip Deselect to Output in High-Z	—	15	—	25	—	25	—	30	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{PU}(2)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(2)	Chip Deselect to Power-Down Time	—	35	—	40	—	50	—	60	ns

3090 tbl 13

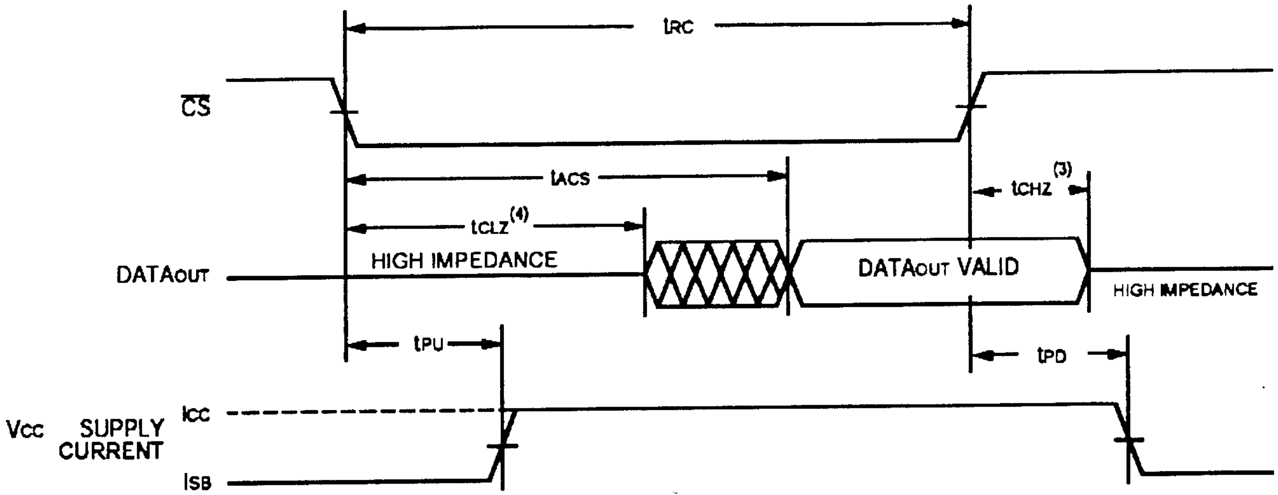
NOTES:
1. –55°C to +125°C temperature range only. Also available 85ns and 100ns devices.
2. This parameter is guaranteed with AC Test load (Figure 2) by device characterization, but is not production tested.

TIMING WAVEFORM OF READ CYCLE NO. 1(1, 2)



3090 drw 07

TIMING WAVEFORM OF READ CYCLE NO. 2[1, 3]



NOTES:
1. WE is HIGH for Read cycle.
2. CS is LOW for Read cycle.
3. Device is continuously selected, CS is LOW.
3. Address valid prior to or coincident with CS transition LOW.
4. Transition is measured ±200mV from steady state.

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	6168SA15		6168SA20/25 6168LA20/25		Unit
		Min.	Max.	Min.	Max.	
Write Cycle						
tWC	Write Cycle Time	15	—	20	—	ns
tCW	Chip Select to End-of-Write	15	—	20	—	ns
tAW	Address Valid to End-of-Write	15	—	20	—	ns
tAS	Address Set-up Time	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	ns
tWR	Write Recovery Time	0	—	0	—	ns
tDW	Data Valid to End-of-Write	9	—	10	—	ns
tDH	Data Hold Time	0	—	0	—	ns
tWHZ(3)	Write Enable to Output in High-Z	—	6	—	7	ns
tOW(3)	Output Active from End-of-Write	0	—	0	—	ns

3090 tbl 14

DATA RETENTION CHARACTERISTICS (LA Version Only)

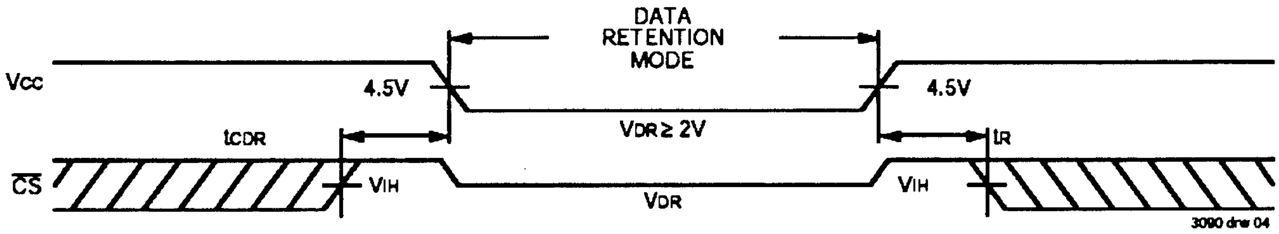
$V_{LC} = 0.2V$, $V_{HC} = V_{CC} - 0.2V$

Symbol	Parameter	Test Condition		IDT6168LA			Unit
				Min.	Typ.(1)	Max.	
V_{DR}	V_{CC} for Data Retention	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		2.0	—	—	V
I_{CCDR}	Data Retention Current		MIL.	—	0.5(2)	100(2)	µA
				—	1.0(3)	150(3)	
			COM'L.	—	0.5(2)	20(2)	µA
				—	1.0(3)	30(3)	
t_{CDR}(5)	Chip Deselect to Data Retention Time			0	—	—	ns
t_R(5)	Operation Recovery Time			t_{RC}(2)	—	—	ns

3090 tbl 10

NOTES:
1. $T_A = +25°C$.
2. at $V_{CC} = 2V$
3. at $V_{CC} = 3V$
4. t_{RC} = Read Cycle Time.
5. This parameter is guaranteed by device characterization, but is not production tested.

LOW Vcc DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
AC Test Load	See Figures 1 and 2

3090 tbl 11

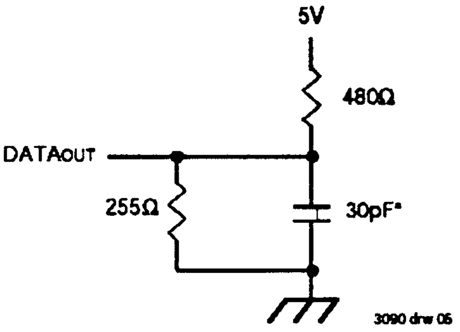


Figure 1. AC Test Load

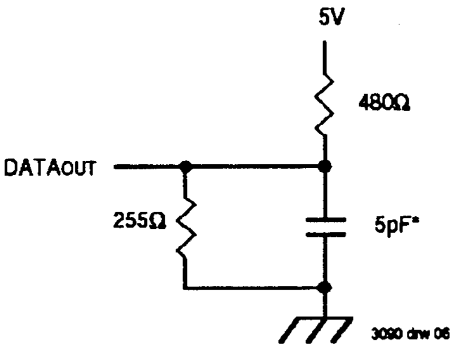


Figure 2. AC Test Load
(for t_{CHZ}, t_{CLZ}, t_{WHZ} and t_{OW})

*Includes scope and jig capacitances

DC ELECTRICAL CHARACTERISTICS(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6168SA15		6168SA20 6168LA20		Unit
			Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = 0(3)	SA	110	120	90	100	mA
		LA	—	—	70	80	
I_{CC2}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	145	165	120	120	mA
		LA	—	—	100	110	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(3)	SA	55	60	45	45	mA
		LA	—	—	30	35	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0(3)	SA	20	20	20	20	mA
		LA	—	—	0.5	5	

3090 tbl 07

DC ELECTRICAL CHARACTERISTICS (CONTINUED)(1)

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	6168SA25 6168LA25		6168SA35 6168LA35		6168SA45/55 6168LA45/55		6168SA70(2) 6168LA70(2)		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC1}	Operating Power Supply Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = 0(3)	SA	90	100	90	100	—	100	—	100	mA
		LA	70	80	70	80	—	80	—	80	
I_{CC2}	Dynamic Operating Current $\overline{CS} \leq V_{IL}$, Outputs Open, V_{CC} = Max., f = f_{MAX}(3)	SA	110	120	100	110	—	110	—	110	mA
		LA	90	100	80	90	—	80	—	80	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \geq V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}(3)	SA	35	45	30	35	—	35	—	35	mA
		LA	25	30	20	25	—	25/20	—	20	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \geq V_{HC}$, V_{CC} = Max., $V_{IN} \geq V_{HC}$ or $V_{IN} \leq V_{LC}$, f = 0(3)	SA	3	10	3	10	—	10	—	10	mA
		LA	0.5	0.3	0.5	0.3	—	0.3	—	0.3	

3090 tbl 08

NOTES:
1. All values are maximum guaranteed values.
2. Also available 85 and 100ns military devices.
3. f_{MAX} = 1/t_{RC}, only address inputs are cycling at f_{MAX}. f = 0 means no address inputs are changing.

DC ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT6168SA		IDT6168LA		Unit
				Min.	Max.	Min.	Max.	
$\lvert I_{LI}\rvert$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL COM'L	— —	10 2	— —	5 2	µA
$\lvert I_{LO}\rvert$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL COM'L	— —	10 2	— —	5 2	µA
V_{OL}	Output LOW Voltage	I_{OL} = 10mA, V_{CC} = Min.		—	0.5	—	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		—	0.4	—	0.4	
V_{OH}	Output HIGH Voltage	I_{OH} = –4mA, V_{CC} = Min.		2.4	—	2.4	—	V

3090 tbl 09

Integrated Device Technology, Inc.

CMOS STATIC RAM
16K (4K x 4-BIT)

IDT6168SA
IDT6168LA

FEATURES:

- High-speed (equal access and cycle time)
  - — Military: 15/20/25/35/45/55/70/85/100ns (max.)
  - — Commercial: 15/20/25/35ns (max.)
- Low power consumption
- Battery backup operation—2V data retention voltage (IDT6168LA only)
- Available in high-density 20-pin ceramic or plastic DIP, 20-pin SOIC, 20-pin CERPACK and 20-pin leadless chip carrier
- Produced with advanced CMOS high-performance technology
- CMOS process virtually eliminates alpha particle soft-error rates
- Bidirectional data input and output
- Military product compliant to MIL-STD-883, Class B

DESCRIPTION:

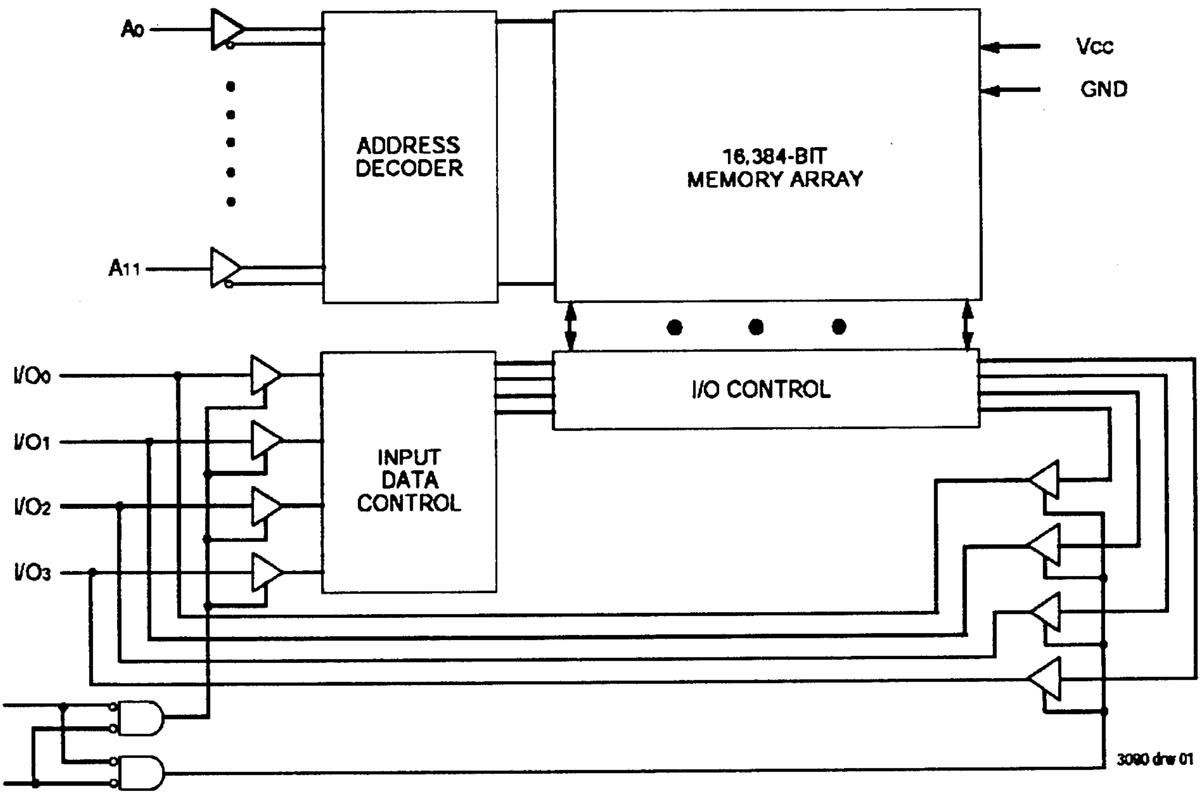
The IDT6168 is a 16,384-bit high-speed static RAM organized as 4K x 4. It is fabricated using IDT's high-performance, high-reliability CMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective approach for high-speed memory applications.

Access times as fast 15ns are available. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes HIGH, the circuit will automatically go to, and remain in, a standby mode as long as $\overline{CS}$ remains HIGH. This capability provides significant system-level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW operating off a 2V battery. All inputs and outputs of the IDT6168 are TTL-compatible and operate from a single 5V supply.

The IDT6168 is packaged in either a space saving 20-pin, 300-mil ceramic or plastic DIP, 20-pin CERPACK, 20-pin SOIC, or 20-pin leadless chip carrier, providing high board-level packing densities.

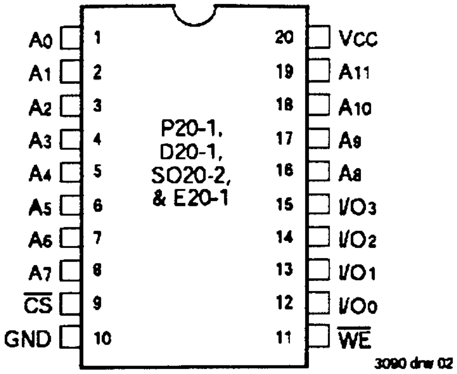
Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM

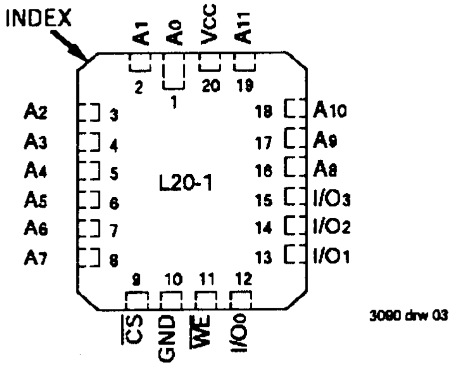


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

PIN CONFIGURATIONS



DIP/SOIC/SOJ/CERPACK
TOP VIEW



LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A_0–A_{11}	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
I/O_{0-3}	Data Input/Output
Vcc	Power
GND	Ground

3090 tbl 01

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
$C_{I/O}$	I/O Capacitance	V_{OUT} = 0V	7	pF

NOTE: 3090 tbl 02

1. This parameter is determined by device characterization, but is not production tested.

TRUTH TABLE[1]

Mode	$\overline{CS}$	$\overline{WE}$	Output	Power
Standby	H	X	High-Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	D_{IN}	Active

NOTE: 3090 tbl 03

1. H = V_{IH}, L = V_{IL}, X = Don't Care

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 3090 tbl 04

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	—	0.8	V

NOTE: 3090 tbl 05

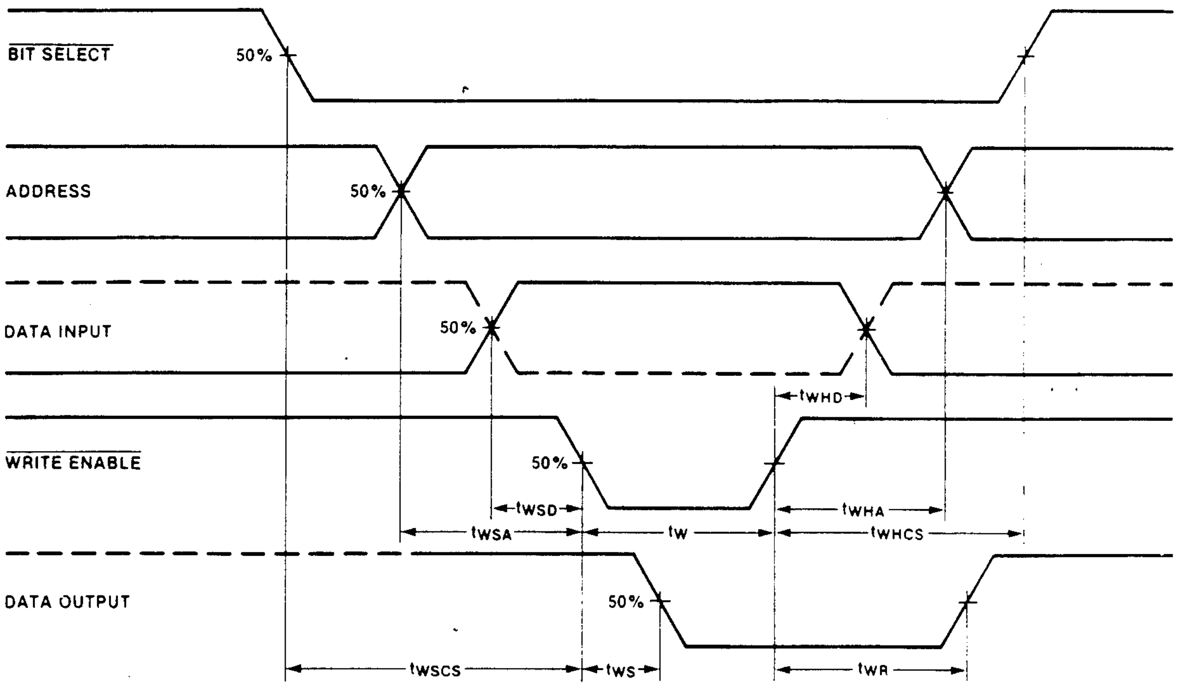
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns, once per cycle.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	VCC
Military	–55°C to +125°C	0V	5V ± 10%
Commercial	0°C to +70°C	0V	5V ± 10%

3090 tbl 06

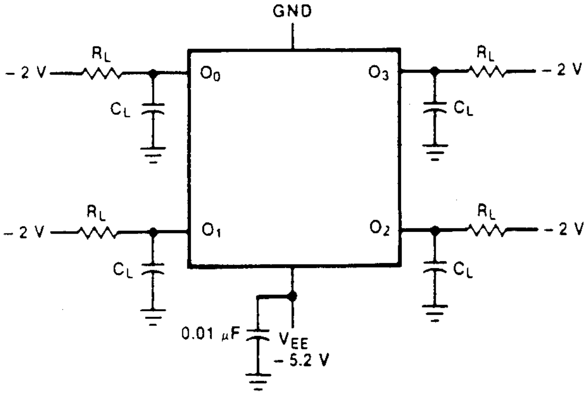
Fig. 4 Write Mode Timing



Note

Timing Diagram represents one solution which results in an optimum cycle time. Timing may be changed to fit various applications as long as the worst case limits are not violated.

Fig. 1 AC Test Circuit



Notes

All Timing Measurements Referenced to 50% of Input Levels

C_L = 30 pF including Fixture and Stray Capacitance

R_L = 50 Ω to −2.0 V

Fig. 2 Input Levels

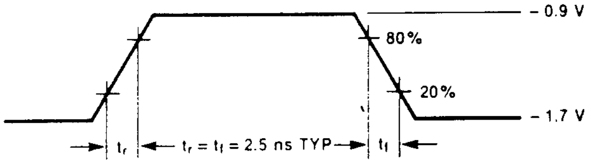
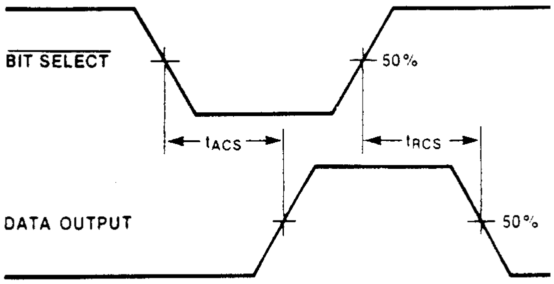
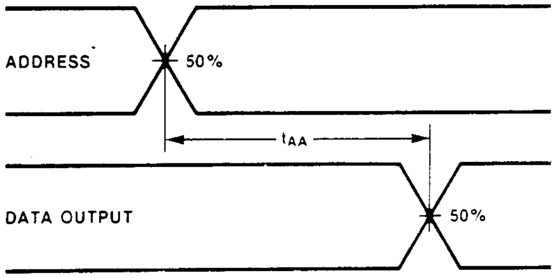


Fig. 3 Read Mode Timing

a Read Mode Propagation Delay from Bit Select



b Read Mode Propagation Delay from Address



DC Characteristics: $V_{EE} = -5.2$ V, $V_{CC} = V_{CCA} =$ GND, $T_A = 0°C$ to $+75°C$ unless otherwise specified[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			220	μA	$V_{IN} = V_{IH(max)}$
I_{IL}	Input LOW Current, $\overline{BS_0}-\overline{BS_3}$ $\overline{WE}$, A_0-A_7, D_0-D_3	0.5 -50		170	μA	$V_{IN} = V_{IL(min)}$
I_{EE}	Power Supply Current	-230	-180		mA	All Inputs and Outputs Open

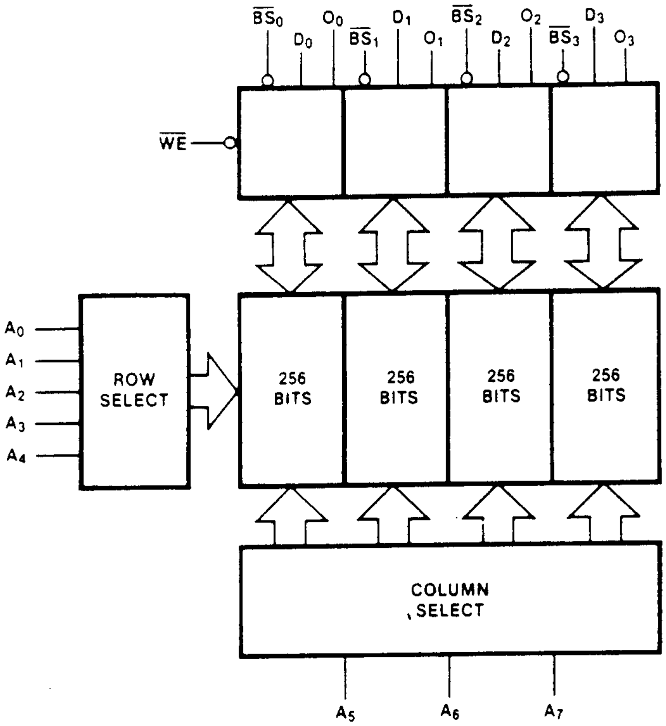
AC Characteristics: $V_{EE} = -5.2$ V ±5%, $V_{CC} = V_{CCA} =$ GND, Output Load = 50 Ω and 30 pF to −2.0 V, $T_A = 0°C$ to $+75°C$

Symbol	Characteristic	Min	Typ	Max	Unit	Condition	
	Read Timing					*Figures 3a, 3b*	Measured at 50% of Input to Valid Output ($V_{IL(max)}$ for V_{OL} or $V_{IH(min)}$ for V_{OH})
t_{ABS}	Bit Select Access Time		3.0	5.0	ns		
t_{RBS}	Bit Select Recovery Time		3.0	5.0	ns		
t_{AA}	Address Access Time[2]		7.0	10	ns		
	Write Timing					$t_{WSA} = 1$ ns *Figure 4*	
t_W	Write Pulse Width to Guarantee Writing	7.0	5.0		ns		
t_{WSD}	Data Setup Time prior to Write	1.0	0		ns		
t_{WHD}	Data Hold Time after Write	2.0	0		ns		
t_{WSA}	Address Setup Time prior to Write	1.0	0		ns	$t_W = 7$ ns *Figure 4*	
t_{WHA}	Address Hold Time after Write	2.0	0		ns		
t_{WSBS}	Bit Select Setup Time prior to Write	1.0	0		ns		
t_{WHBS}	Bit Select Hold Time after Write	2.0	0		ns		
t_{WS}	Write Disable Time		3.0	5.0	ns		
t_{WR}	Write Recovery Time		6.0	12	ns		
t_r	Output Rise Time		3.0		ns	Measured between 20% and 80% or 80% and 20%, *Figure 2*	
t_f	Output Fall Time		3.0		ns		
C_{IN}	Input Pin Capacitance		4.0	5.0	pF	Measured with a Pulse Technique	
C_{OUT}	Output Pin Capacitance		7.0	8.0	pF		

[1] See Family Characteristics for other dc specifications.

[2] The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern

Logic Diagram



Functional Description

The F10422 is a fully decoded 1024-bit read/write random access memory, organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 through A_7.

Four Bit Select inputs are provided for logic flexibility. For larger memories, the fast bit select access time permits the decoding of individual bit selects from the address without increasing address access time.

The read and write operations are controlled by the state of the active-LOW Write Enable ($\overline{WE}$) input. With $\overline{WE}$ held LOW and the bit selected, the data at $D_0 - D_3$ is written into the addressed location. Since the write function is level triggered, data must be held stable for at least $t_{WSD(min)}$ plus $t_{W(min)}$ to insure a valid write. To read, $\overline{WE}$ is held HIGH and the bit selected. Non-inverted data is then presented at the output (O).

The outputs of the F10422 are unterminated emitt followers, which allow maximum flexibility in choc output connection configurations. In many applic it is desirable to tie the outputs of several F10422 devices together to allow easy expansion. In other applications the wired-OR need not be used. In ei case an external 50 Ω pull-down resistor to −2 V o equivalent network must be used to provide a LO the output.

Truth Table

Inputs			Outputs	Mo
$\overline{BS}_n$	$\overline{WE}$	D_n	O_n	
H	X	X	L	Not S
L	L	L	L	Write
L	L	H	L	Write
L	H	X	Data	Read

Each bit has independent $\overline{BS}$, D, and O, but all have common $\overline{WE}$

L = LOW Voltage Levels = −1.7 V (Nominal)

H = HIGH Voltage Levels = −0.9 V (Nominal)

X = Don't Care

Data = Previously stored data

F10422
256 x 4-Bit Static Random Access Memory

F10K ECL Product

Description

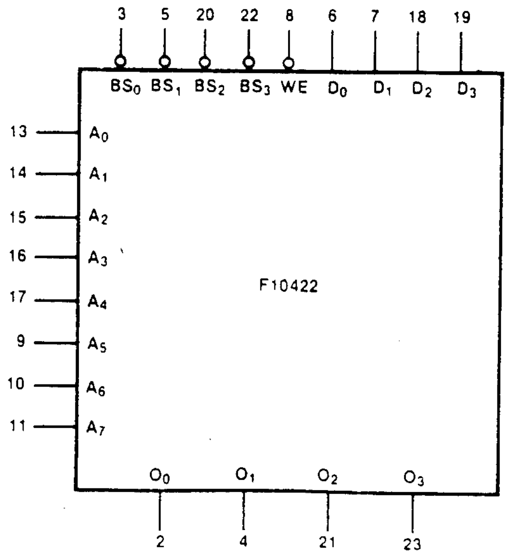
The F10422 is a 1024-bit read/write Random Access Memory (RAM), organized 256 words by four bits per word. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as four active-LOW Bit Select lines.

- **Address Access Time-10 ns Max**
- **Bit Select Access Time-5.0 ns Max**
- **Four Bits Can be Independently Selected**
- **Open-emitter Outputs for Easy Memory Expansion**
- **Power Dissipation-0.92 mW/Bit Typ**
- **Power Dissipation Decreases with Increasing Temperature**

Pin Names

$\overline{WE}$	Write Enable Input (Active LOW)
$\overline{BS}_0$-$\overline{BS}_3$	Bit Select Inputs (Active LOW)
A_0-A_7	Address Inputs
D_0-D_3	Data Inputs
O_0-O_3	Data Outputs

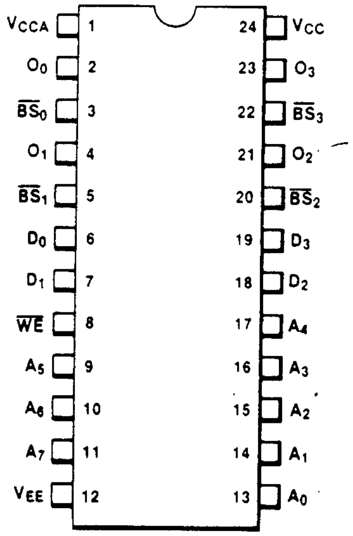
Logic Symbol



V_{CC} = Pin 24
V_{CCA} = Pin 1
V_{EE} = Pin 12

Connection Diagrams

24-Pin DIP (Top View)



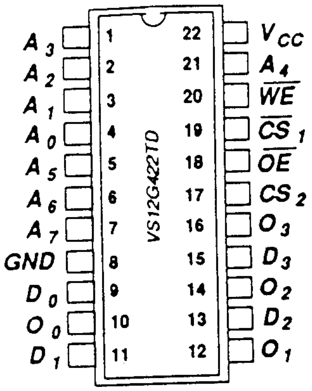
Note

The 24-pin flatpak version has the same pinout connections as the Dual In-Line package

Ordering Information (See Section 5)

Package	Outline	Order Code
Ceramic DIP	6Y	DC
Flatpak	4V	FC

Connection Diagram (22-pin DIP - Top View)

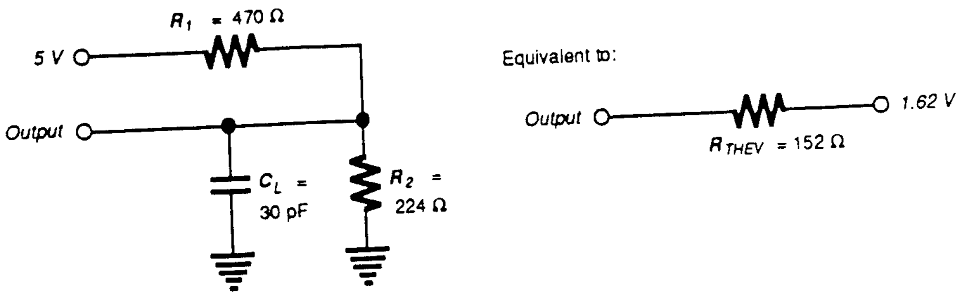


Pin Description

Pin #	Name	I/O	Description
1-7, 21	A_0 - A_7	I	Address inputs
9, 11, 13, 15	D_0 - D_3	I	Data Inputs
19	$\overline{CS}_1$	I	Chip select input (Active LOW)
10, 12, 14, 16	O_0 - O_3	O	Data outputs
17	CS_2	I	Chip select input (Active HIGH)
20	$\overline{WE}$	I	Write enable input (Active LOW)
18	$\overline{OE}$	I	Output enable input (Active LOW)
22	V_{CC}		5.0 V supply connection
8	GND		Ground connection (0 V)

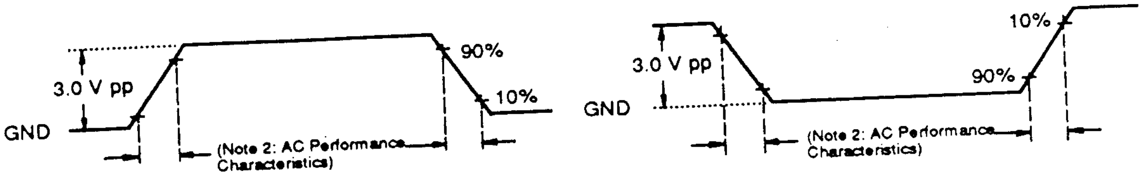
AC Test Loading Condition *(Figure 1)*

The following conditions apply to the "AC Performance Characteristics" indicated on pages 4-3 and 4-4.



AC Test Input Levels *(Figure 2)*

The following conditions apply to the "AC Performance Characteristics" indicated on pages 4-3 and 4-4.



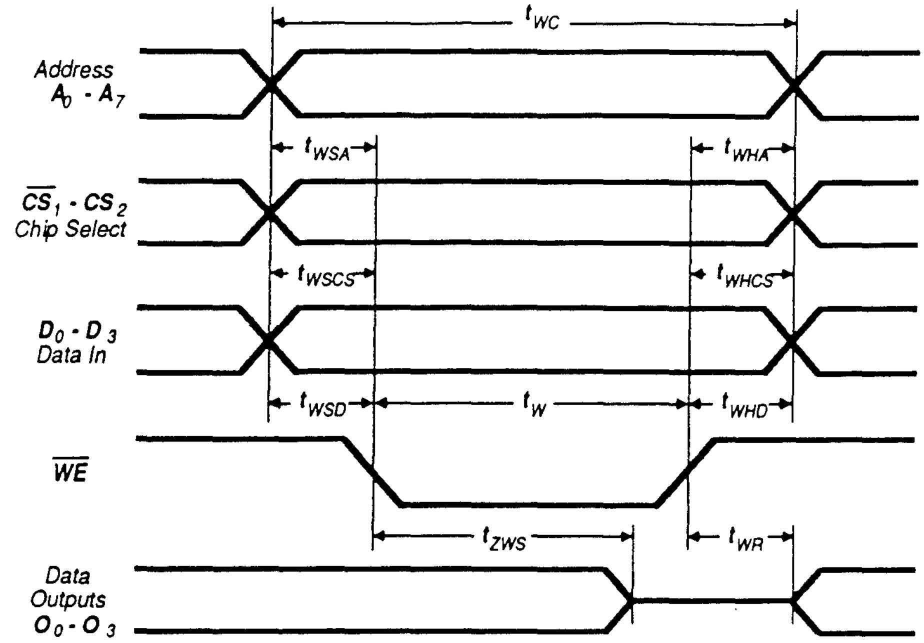
Address Designators

Address Name	Address Function	Pin Number	
		22-pin DIP	28-pin LCC
A_0	AX_0	4	21
A_1	AX_1	3	20
A_2	AX_2	2	19
A_3	AX_3	1	17
A_4	AX_4	21	16
A_5	AY_5	5	22
A_6	AY_6	6	23
A_7	AY_7	7	24

AC Performance Characteristics - continued (1)

(Over guaranteed operating conditions, GND = 0 V)

2. Write Mode:



Paramters	Description	6 ns		5 ns		4ns		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write cycle time	6	—	5	—	4	—	ns
t_{ZWS} (2)	Write disable to HIGH Z	—	5	—	4	—	3.5	ns
t_{WR}	Write recovery time	—	4.5	—	3.5	—	3	ns
t_W (3)	Write pulse width	4	—	3	—	2.5	—	ns
t_{WSD}	Data setup time prior to write	0	—	0	—	0	—	ns
t_{WHD}	Data hold time after write	2	—	2	—	1.5	—	ns
t_{WSA} (3)	Address setup time	0	—	0	—	0	—	ns
t_{WHA}	Address hold time	2	—	2	—	1.5	—	ns
t_{WSCS}	Chip select setup time	0	—	0	—	0	—	ns
t_{WHCS}	Chip select hold time	2	—	2	—	1.5	—	ns

Notes: 1) Test conditions assume signal transition times of 3 ns or less. Timing reference levels of 1.5 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance as in figure 1 on page 4-5

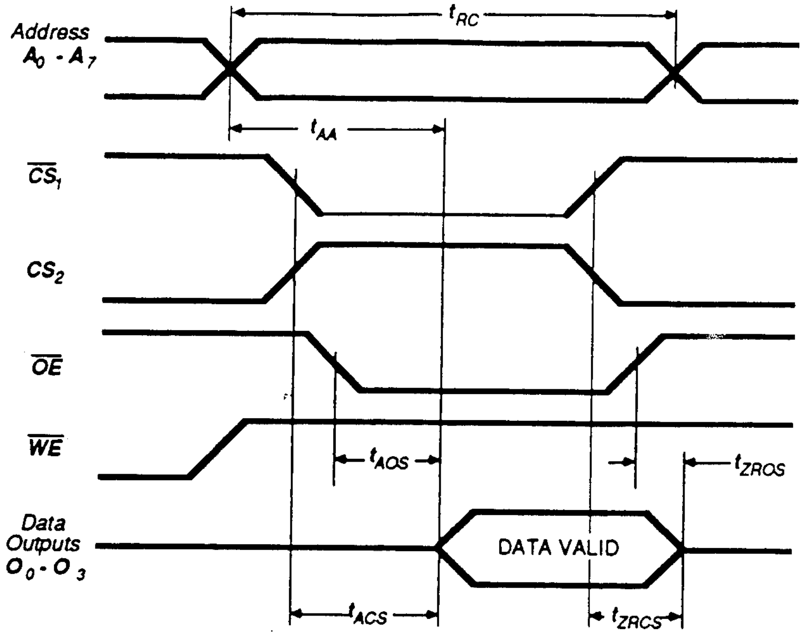
2) Transition is measured at steady state HIGH level -250 mV or steady state LOW level +250 mV on the output from 1.5 V level on the input with load shown in figure 1 on page 4-5

3) t_W measured at t_{WSA} = min; t_{WSA} measured at t_W = min

AC Performance Characteristics (1)

(Over guaranteed operating conditions, GND = 0 V)

1. Read Mode:



Parameters	Description	6 ns		5 ns		4 ns		Units
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read cycle time	6	—	5		4		ns
t_{ACS}	Chip select time	—	4	—	3.5		2.5	ns
t_{ZRCS} (2)	Chip select to HIGH Z	—	5	—	4		3.5	ns
t_{AOS}	Output enable time	—	4	—	3.5		2.5	ns
t_{ZROS} (2)	Output enable to HIGH Z	—	5	—	4		3.5	ns
t_{AA}	Address access time	—	6	—	5		4	ns

Notes: 1) *Test conditions assume signal transition times of 3 ns or less. Timing reference levels of 1.5 V and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance as in figure 1 on page 4-5*

2) *Transition is measured at steady state HIGH level -250 mV or steady state LOW level +250 mV on the output from 1.5 V level on the input with load shown in figure 1 on page 4-5*

Truth Table

Inputs				Output	Mode
$\overline{OE}$	$\overline{CS}_1$	CS_2	$\overline{WE}$		
X	H	X	X	HIGH Z	Not Selected
X	X	L	X	HIGH Z	Not Selected
L	L	H	H	D_{OUT}	READ
X	L	H	L	HIGH Z	WRITE
H	X	X	X	HIGH Z	Output Disabled

H = HIGH Voltage Level (2.4 V) *X = Don't Care (HIGH or LOW)*
L = LOW Voltage Level (0.4 V) *HIGH Z = High-Impedence*

Absolute Maximum Ratings (1)

Power Supply Voltage (V_{CC})	-0.5 V to +6.0 V
Input Voltage Applied, (V_{IN})	-1.0 V to +7.0 V
Input Current, (I_{IN}), (DC, output LOW)	-30 to +30 mA
Output Current, (I_{OUT}), (DC, output LOW)	20 mA
Maximum Junction Temperature, (T_j)	150°C
Case Temperature Under Bias, (T_C)	-55° to +125°C
Storage Temperature(2), (T_{STG})	-65° to +150°C

Recommended Operating Conditions

Power Supply Voltage, (V_{CC})	4.75 to 5.25 V
Operating Temperature Range (2)	0° to +70°C

NOTES: (1) CAUTION: Stresses listed under "Absolute Maximum Ratings" may be applied to devices one at a time without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

(2) Both lower and upper limits of specification are case temperatures.

DC Characteristics *(Over recommended operating conditions)*

Parameters	Description	Commercial Range				Test Conditions
		5,6 ns		4 ns		
		Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	2.4 V	—	2.4 V	—	V_{CC} = MIN, I_{OH} = -5.2 mA
V_{OL}	Output LOW voltage	—	0.5 V	—	0.5 V	V_{CC} = MIN, I_{OL} = 8.0 mA
V_{IH}	Input HIGH voltage	2.0 V	—	2.0 V	—	
V_{IL}	Input LOW voltage	—	0.8 V	—	0.8 V	
I_{IX}	Input LOAD current	-100 µA	100 µA	-100 µA	100 µA	GND $\leq V_{IN} \leq V_{CC}$
V_{CD}	Input diode clamp voltage (1)	-1.0 V	V_{CC}+1	-1.0 V	V_{CC}+1	I_{IN} = ± 30 mA
I_{OZ}	Output current (HIGH-Z)	-1.0 mA	1.0 mA	-1.0 mA	1.0 mA	$V_{OL} \leq V_{OUT} \leq V_{OH}$ *Output Disabled*
I_{CC}	Power supply current (from V_{CC})	—	250 mA	—	350 mA	V_{CC} = MAX, I_{OUT} = 0 mA

Notes: (1) Clamped by input Schottky diodes to GND and V_{CC}

VS12G422T

256 x 4 Static RAM

Features

- 256 words by 4-bit static RAM for cache and control store applications
- Very fast: Choice of 4, 5, and 6 ns maximum address access times
- TTL compatible inputs and outputs
- Single +5.0 Volt power supply
- Very low sensitivity to radiation
- Standard 22-pin DIP
- Fully static operation - equal access and cycle times
- Pin compatible with standard silicon -422 and -122 products

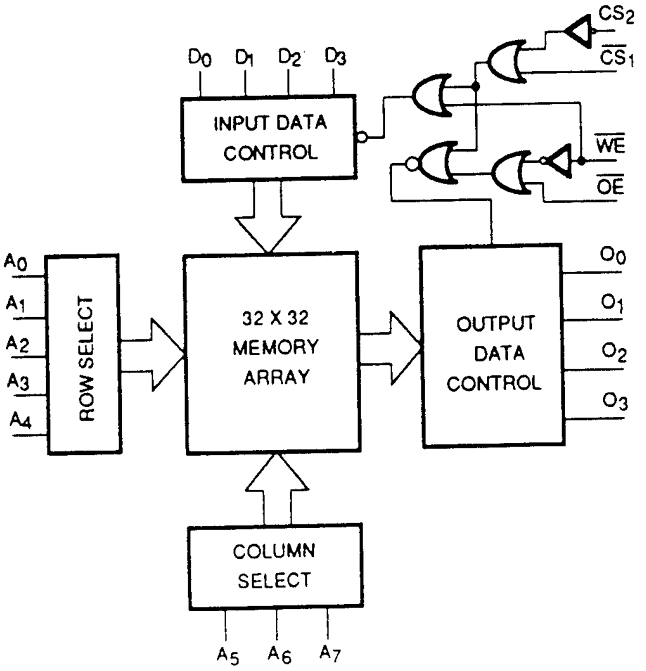
Functional Description

The Vitesse VS12G422T is a very high speed, fully decoded 1024-bit read write static random access memory organized as 256 words by 4 bits. All inputs and outputs of this RAM is TTL compatible and operation is from a standard +5.0 Volt power supply.

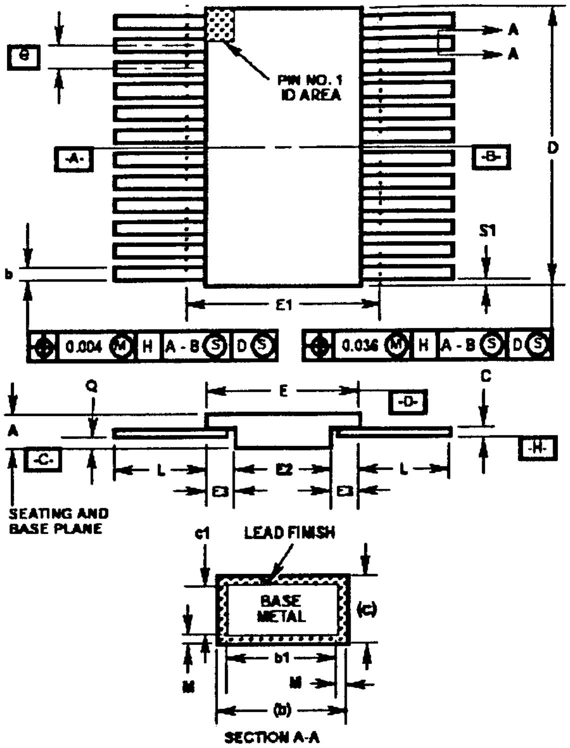
Fully static asynchronous internal circuits are used, which require no clocks or refreshing for operation. Memory expansion is provided by an active LOW chip select input ($\overline{CS}_1$), an active HIGH chip select input (CS_2) and three-state outputs. Due to its static operation, the VS12G422T offers equal read and write cycle times, which further simplifies system design. This RAM is packaged in a standard 22-pin DIP. Refer to Section 6, "Packaging" for a complete description of this package.

The high speed and standard pinout of the VS12G422Tmakes it ideal for both existing and new designs in cache memory, signal processing, and video applications where access time is the critical parameter. The low sensitvity to radiation of this product makes it highly suitable for aerospace applications where high radiation tolerance is necessary. The VS12G422T is fabricated in gallium arsenide using the Vitesse H-GaAs™ E/D MESFET process which achieves high speed and low power dissipation.

Block Diagram



Packaging



K36.A

36 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.138	-	3.51	-
b	0.006	0.013	0.15	0.33	-
b1	0.006	0.010	0.15	0.25	-
c	0.004	0.011	0.10	0.28	-
c1	0.004	0.008	0.10	0.20	-
D	0.620	0.640	15.75	16.26	3
E	0.620	0.640	15.75	8.64	-
E1	-	0.660	-	16.76	3
E2	0.470	0.490	11.94	12.45	-
E3	0.030	-	0.76	-	7
e	0.025 BSC		0.64 BSC		-
k	-	-	-	-	-
L	0.240	0.280	6.10	7.11	-
Q	0.026	0.045	0.66	1.14	8
S1	-	-	-	-	-
M	-	0.0015	-	0.04	-
N	36		36		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Metallization Topology

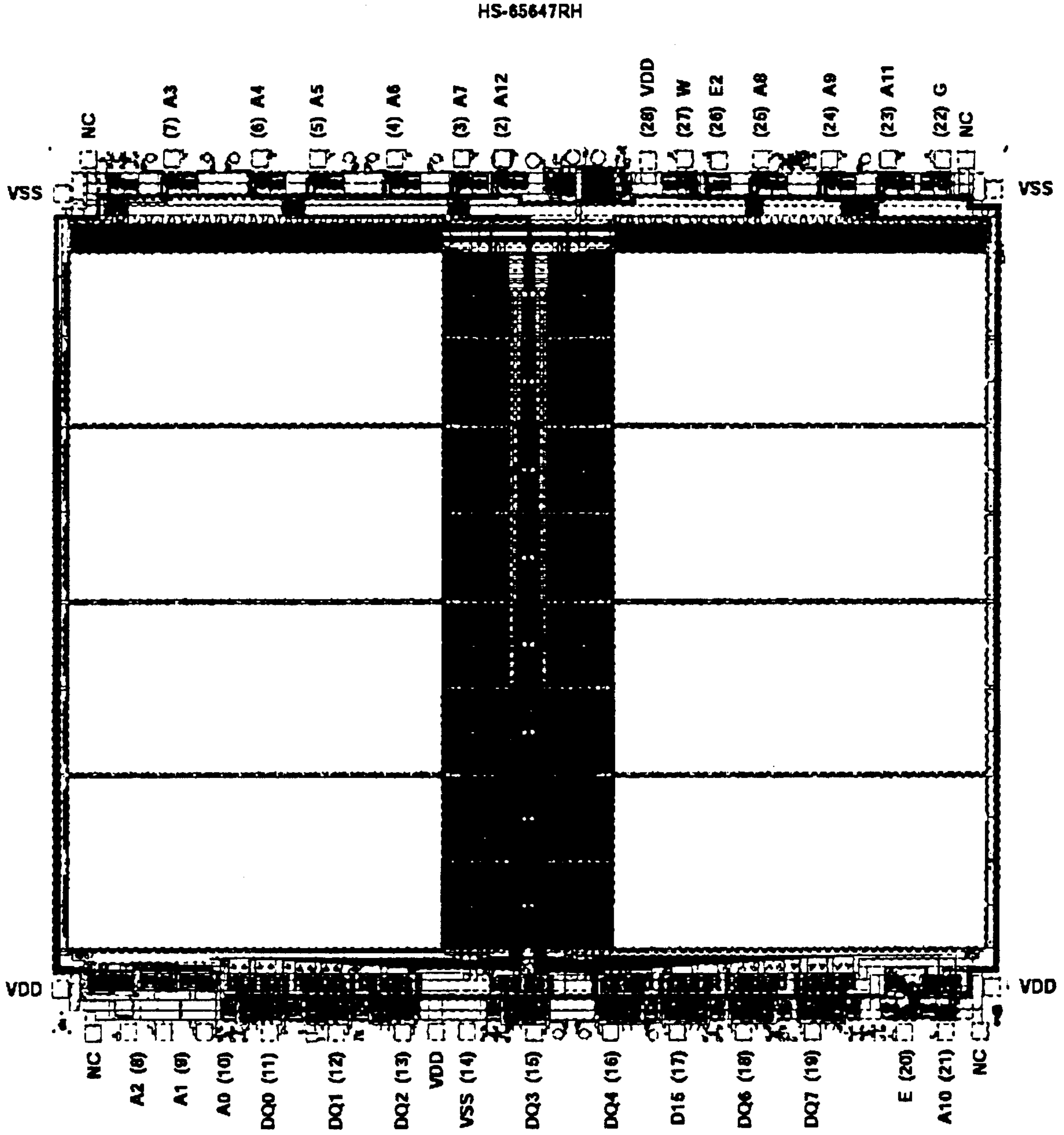
DIE DIMENSIONS:
313 x 291 x 21 ±1mils

METALLIZATION:
Type: Al/Si/Cu
Metal 1 Thickness: 7500Å ± 2kÅ
Metal 2 Thickness: 10kÅ ± 2kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

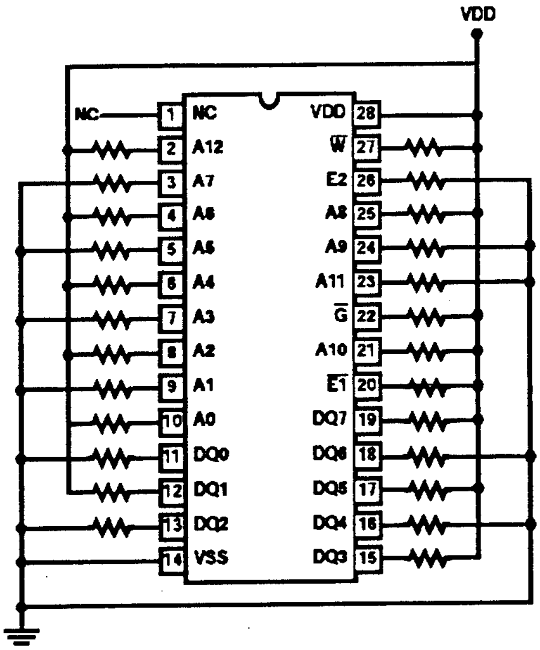
WORST CASE CURRENT DENSITY:
1.5 x 10^5 Amps/cm^2

Metallization Mask Layout



Irradiation Circuit

HS-65647RH (8K x 8 TSOS4 SRAM) 28 LEAD CERAMIC DIP



NOTES:

1. VDD = 5.5V ± 0.5V
   R = 10kΩ ± 10%
2. Group E sample size is two die/wafer.

Test Patterns

MARCH (II)PATTERN

After a background of zeros is written, each cell (from beginning to end in sequence) is read, written to a one and reread. When the array is full of ones each cell (from the end to the beginning) is read, restored to a zero and reread.

After this the pattern is repeated but with complemented data.

MASEST PATTERN (Multiple Address Select Pattern)

A checkerboard pattern is written into the memory. Then the first cell is read, then its binary address complement is read. The second cell is read and then its binary address complement is read. This pattern of incrementing the address and then reading its binary address complement is repeated until the entire memory is read.

This is then repeated but using a checkerboard bar pattern.

GALROW PATTERN (Row Galloping Pattern)

After a background of zeros is written into the memory a one is written into the first cell. It is then read alternately with each other cell in the row. The test cell is then rewritten back to a zero. The test cell is then incremented and the sequence is repeated until all cells in the memory have been used as a test cell.

This is pattern then repeated but using complemented data.

GALCOL PATTERN (Column Galloping Pattern)

After a background of zeros is written into the memory a one is written into the first cell. It is then read alternately with each other cell in the column. The test cell is then rewritten back to a zero. The test cell is then incremented and the sequence is repeated until all cells in the memory have been used as a test cell.

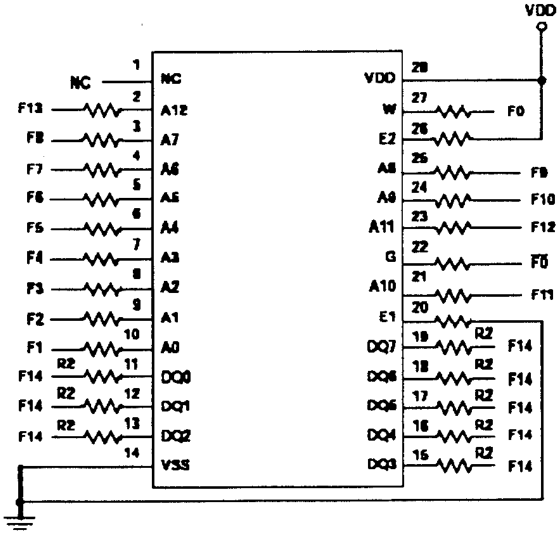
This is pattern then repeated but using complemented data.

CHECKERBOARD PATTERN and CHECKERBOARD BAR

A checkerboard is written (101010) into the memory and then the pattern is read back. This is then repeated but using complemented data.

Burn-In Circuits

HS-65647RH 28 LEAD FLATPACK AND CERAMIC DIP

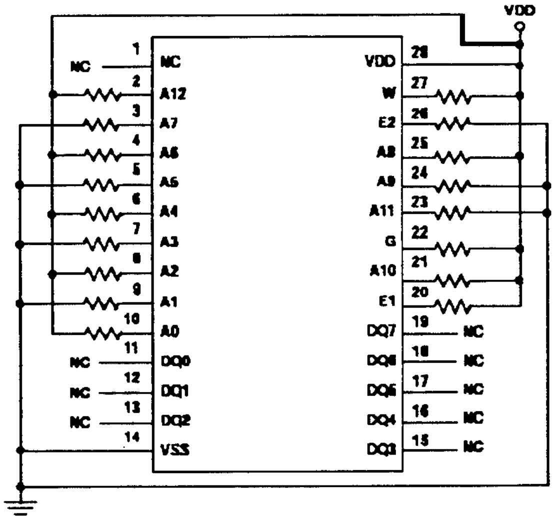


DYNAMIC CONFIGURATION

NOTES:

1. VDD = 5.5V Min
2. R = 10kΩ ± 10%, except R2 = 47kΩ ± 10%
3. VIH: VDD ± 0.5V, VIL: 0.4V ± 0.4V
4. F0 = 100kHz ± 10%, 50% Duty Cycle
5. F1 = F0/2; F2 = F1/2; F3 = F2/2; . . . F14 = F13/2
6. $\overline{F0}$ = Inverted F0

HS-65647RH 28 LEAD FLATPACK AND CERAMIC DIP

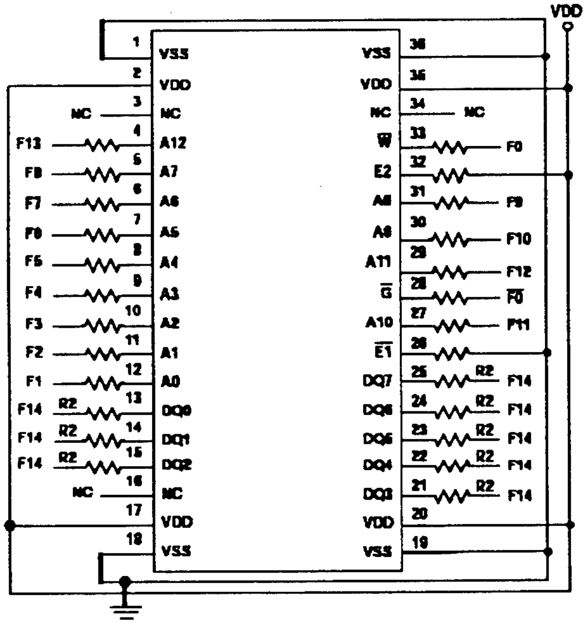


STATIC CONFIGURATION

NOTES:

1. VDD = 5.5V Min
2. R = 10kΩ ± 10%

HS-65647RH 36 LEAD FLATPACK

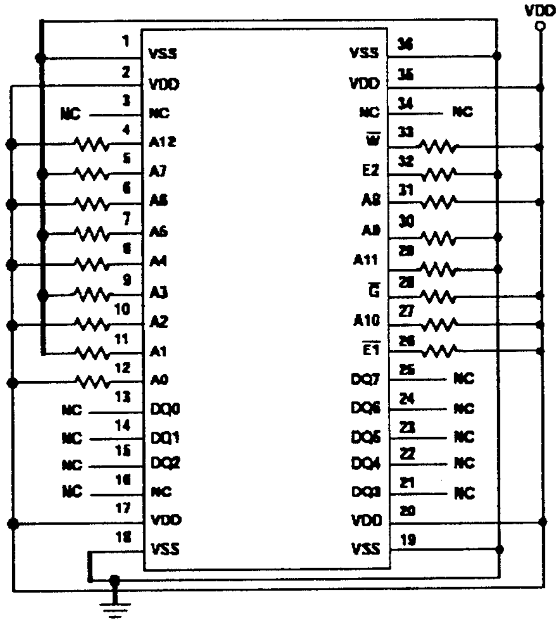


DYNAMIC CONFIGURATION

NOTES:

1. VDD = 5.5V Min
2. R = 10kΩ ± 10%, except R2 = 4.7kΩ ± 10%
3. VIH: VDD ± 0.5V, VIL: 0.4V ± 0.4V
4. F0 = 100kHz ± 10%, 50% Duty Cycle
5. F1 = F0/2; F2 = F1/2; F3 = F2/2; . . . F14 = F13/2
6. $\overline{F0}$ = Inverted F0

HS-65647RH 36 LEAD FLATPACK



STATIC CONFIGURATION

NOTES:

1. VDD = 5.5V Min
2. R = 10kΩ ± 10%

Performance Curves

HS-65647RH TYPICAL PERFORMANCE CHARACTERISTICS
T_A = +25°C, Unless Otherwise Specified

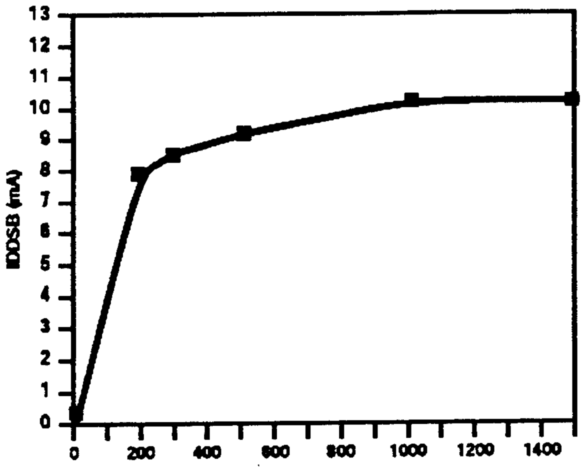


FIGURE 6

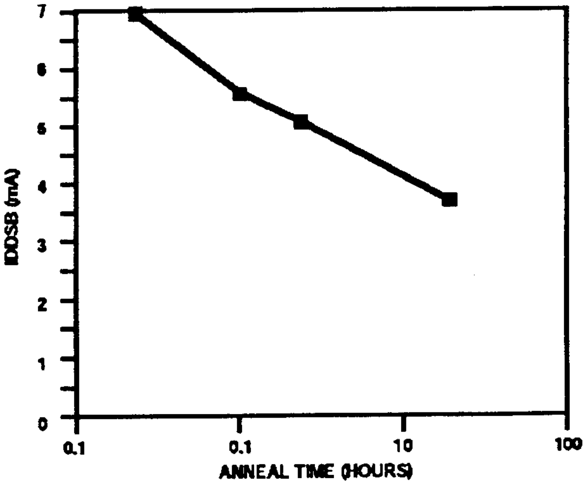


FIGURE 7

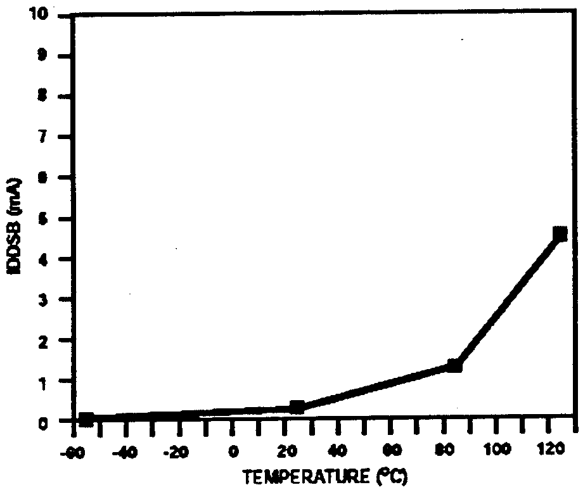


FIGURE 8

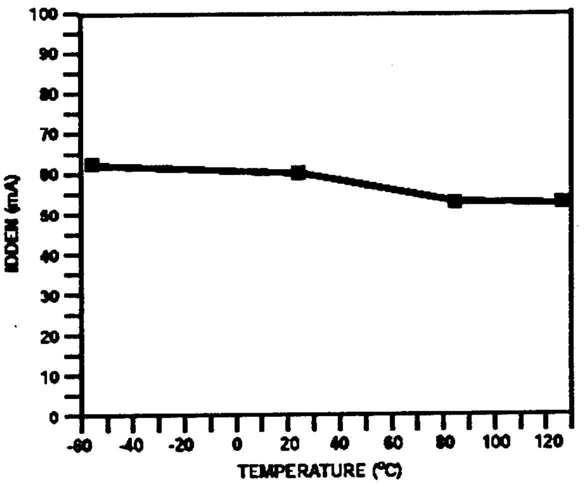


FIGURE 9

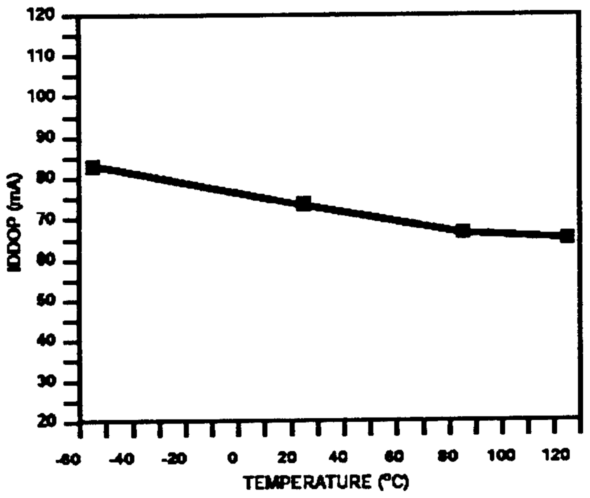


FIGURE 10

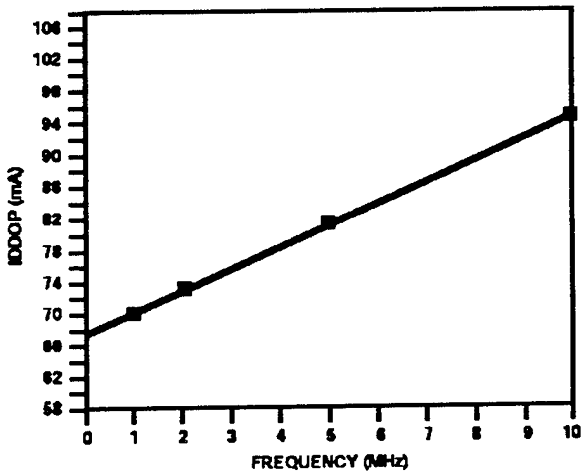


FIGURE 11

Timing Waveforms (Continued)

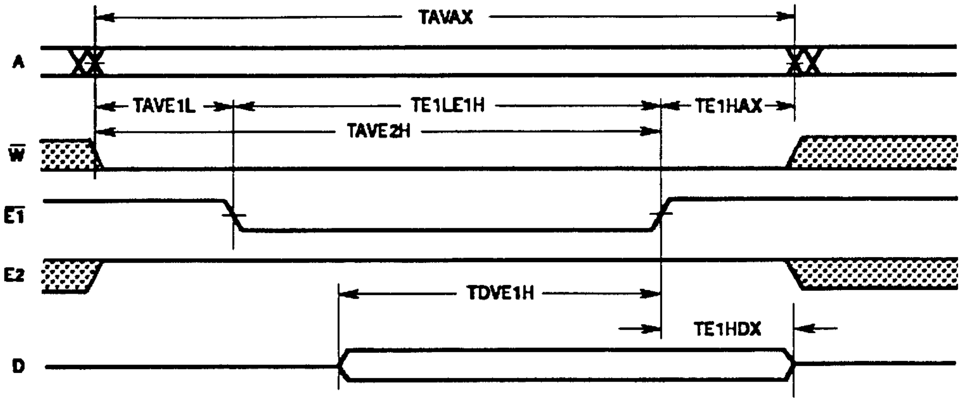


FIGURE 4. WRITE CYCLE II: EARLY WRITE - CONTROLLED BY $\overline{E1}$

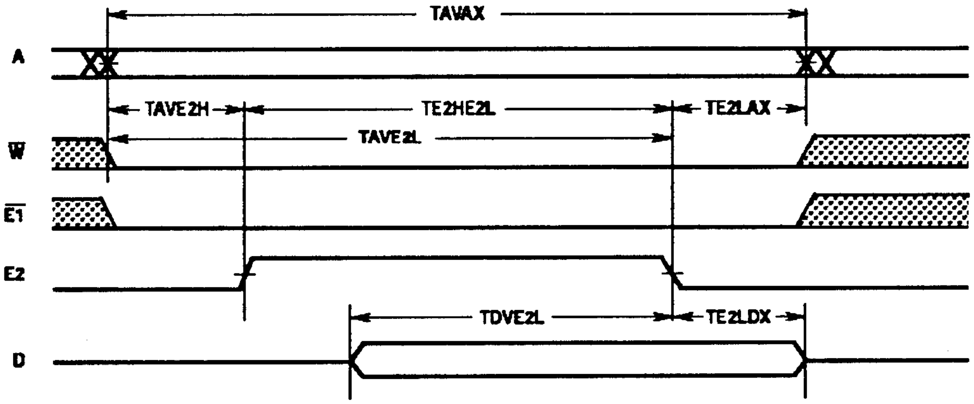


FIGURE 5. WRITE CYCLE III: EARLY WRITE - CONTROLLED BY E2

Timing Waveforms

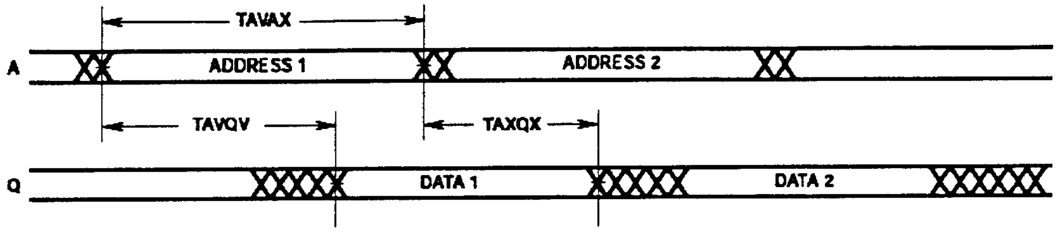


FIGURE 1. READ CYCLE I: $\overline{W}$, E2 HIGH; $\overline{G}$, $\overline{E1}$ LOW

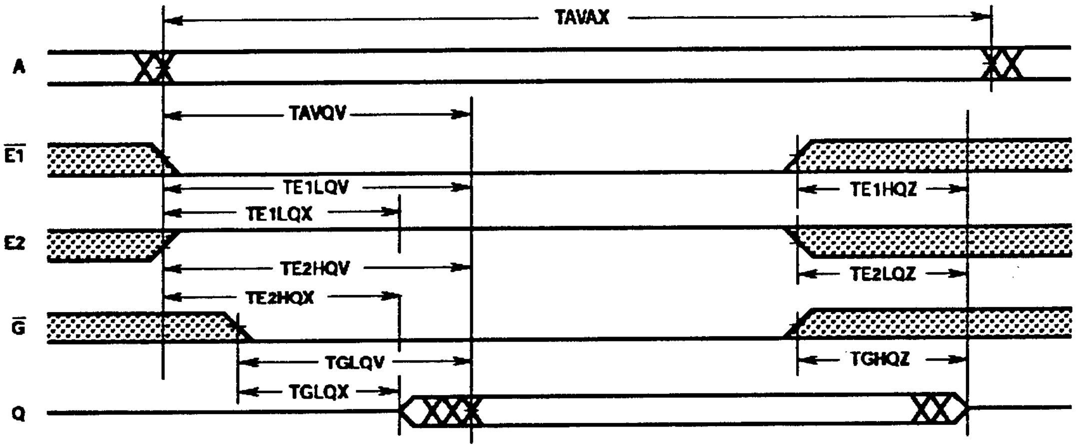


FIGURE 2. READ CYCLE II: $\overline{W}$ HIGH

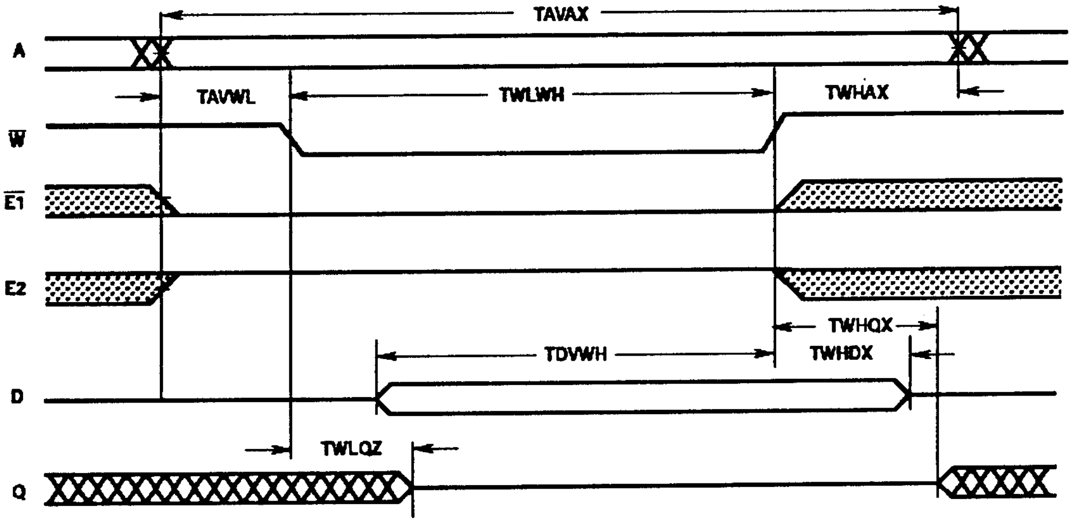


FIGURE 3. WRITE CYCLE I: LATE WRITE

Harris Space Level Product Flow -8

GAMMA Radiation Verification (Each Wafer) Method 1019, 2 Samples/Wafer, 0 Rejects

Periodic- Wire Bond Pull Monitor, Method 2011

Periodic- Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition B

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% External Visual

100% Initial Electrical Test

100% Dynamic Burn-In, Condition D, 160 Hours, +125°C or Equivalent, Method 1015

100% Interim Electrical Test

100% PDA, Method 5004 (Note 1)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 2)

Sample - Group B, Method 5005 (Note 3)

Sample - Group C, Method 5005 (Notes 3 and 4)

Sample - Group D, Method 5005 (Notes 3 and 4)

100% Data Package Generation (Note 5)

NOTES:

1. Failures from subgroup 1, 7 are used for calculating PDA. The maximum allowable PDA = 5%.
2. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
3. Group B, C and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B Test, Group C Test, Group C Samples, Group D Test and Group D Samples.
4. Group C and/or Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group C Generic Data and/or Group D Generic Data. Generic data is not guaranteed to be available and is therefore not available in all cases.
5. Data Package Contents:
    - Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
    - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
    - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
    - Group B, C and D attributes and/or Generic data is included when required by the P.O.
    - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

Harris Space Level Product Flow -Q

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 2 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 72 Hours Min, +125°C Min, Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% PDA 1, Method 5004 (Note 1)

100% Dynamic Burn-In, Condition D, 240 Hours, +125°C or Equivalent, Method 1015

100% Interim Electrical Test 2(T2)

100% Delta Calculation (T0-T2)

100% PDA 2, Method 5004 (Note 1)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic (X-Ray), Method 2012 (Note 2)

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 3)

Sample - Group B, Method 5005 (Note 4)

Sample - Group D, Method 5005 (Notes 4 and 5)

100% Data Package Generation (Note 6)

NOTES:

1. Failures from subgroup 1, 7 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
2. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
3. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
4. Group B and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B Test, Group Samples, Group D Test and Group D Samples.
5. Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group D Generic Data. Generic data is not guaranteed to be available and is therefore not available in all cases.
6. Data Package Contents:
    - Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
    - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
    - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
    - X-Ray report and film. Includes penetrometer measurements.
    - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
    - Lot Serial Number Sheet (Good units serial number and lot number).
    - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
    - Group B and D attributes and/or Generic data is included when required by the P.O.
    - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C), GROUP B, SUBGROUP 5

PARAMETER	SYMBOL	DELTA LIMITS
Standby Supply Current	IDDSB	±150µA
High Impedance Output Leakage Current	IOZH, IOZL	± 2µA
Input Leakage Current	IIH, IIL	± 150nA
Low Level Output Voltage	VOL	± 60mV
Output High Voltage	VOH	± 150mV

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS			
		TESTED FOR -Q	RECORDED FOR -Q	TESTED FOR -8	RECORDED FOR -8
Initial Test	100% 5004	1, 7, 9	1 (Note 2)	1, 7, 9	
Interim Test	100% 5004	1, 7, 9, Δ	1, Δ (Note 2)	1, 7, 9	
PDA	100% 5004	1, 7, Δ	-	1, 7	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	-	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Subgroup B5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Δ	1, 2, 3, Δ (Note 2)	N/A	
Subgroup B6	Sample 5005	1, 7, 9	-	N/A	
Group C	Sample 5005	N/A	N/A	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group D	Sample 5005	1, 7, 9	-	1, 7, 9	
Group E, Subgroup 2	Sample 5005	1, 7, 9	-	1, 7, 9	

NOTES:

1. Alternate Group A testing in accordance with MIL-STD-883 method 5005 may be exercised.
2. Table 5 parameters only

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Write Enable High to Output ON	TWHQX	VDD = 4.5V and 5.5V	1	$-55^{\circ}C \le T_A \le +125^{\circ}C$	0	-	ns
Chip Enable to Output ON	TE1LQX TE2HQX	VDD = 4.5V and 5.5V	1	$-55^{\circ}C \le T_A \le +125^{\circ}C$	0	-	ns
Output Enable to Output ON	TGLQX	VDD = 4.5V and 5.5V	1	$-55^{\circ}C \le T_A \le +125^{\circ}C$	0	-	ns
Chip Enable to Output in High Z	TE1HQZ TE2LQZ	VDD = 4.5V and 5.5V	1	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	15	ns
Output Disable to Output in High Z	TGHQZ	VDD = 4.5V and 5.5V	1	$-55^{\circ}C \le T_A \le +125^{\circ}C$	-	15	ns
Output Hold from Address Change	TAXQX	VDD = 4.5V and 5.5V	1	$-55^{\circ}C \le T_A \le +125^{\circ}C$	0	-	ns

NOTES:

1. The parameters listed are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. Applies to DIP device types only.
3. Applies to Flatpack device types only.
4. All measurements referenced to device GND.

TABLE 4. POST 300K RAD DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Standby Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, $\overline{E1}$ = VDD, E2 = 0V, VI = VDD or GND	+25°C	-	10	mA
Enabled Supply Current	IDDEN	VDD = 5.5V, IO = 0mA, $\overline{E1}$ = 0.0V, E2 = VDD, VI = VDD or GND	+25°C	-	82	mA
Operating Supply Current (Note 2)	IDDOP	VDD = 5.5V, IO = 0mA, f = 2MHz, $\overline{E}$ = 0V,VI = VDD or GND	+25°C	-	100	mA
Data Retention Supply Current	IDDDR	VDD = 2.0V, IO = 0mA, $\overline{E}$ = VDD	+25°C	-	6	mA

NOTES:

1. DC parameters not listed in this table are tested at the +25°C pre-irradiation test limits. All AC parameters are tested at the +25°C pre-irradiation test limits.
2. Typical IDDOP derating = 3mA/MHz (3mA increase in IDDOP per 1MHz increase in address frequency.)

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Address Access Time	TAVQV	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	-	50	ns
Output Enable Access Time	TGLQV	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	-	15	ns
Chip Enable Access Time	TE1LQV TE2HQV	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	-	50	ns
Write Recovery Time	TWHAX TE1HAX TE2LAX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	0	-	ns
Chip Enable to End-of-Write	TE1LE1H TE2HE2L	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	35	-	ns
Address Setup Time	TAVWL TAVE1L TAVE2H	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	5	-	ns
Write Enable Pulse Width	TWLWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	25	-	ns
Data Setup Time	TDVWH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	30	-	ns
	TDVE1H TDVE2L	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	30	-	ns
Data Hold Time	TWHDX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	0	-	ns
Address Hold Time	TAVE1H TAVE2L	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	40	-	ns
	TE2LDX TE1HDX	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +85°C, +125°C	0	-	ns

NOTES:

1. AC measurements tested at worst case VDD. Guaranteed over full operating range.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to VDD; timing reference levels = 2.0V; output load = 1 TTL equivalent load and CL ≥ 50pF, for CL > 50pF, access times are derated 0.15ns/pF.
3. For timing waveforms, see Low Voltage Data Retention and Read/Write Cycles.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CIN	VDD = Open, f = 1MHz	1, 2, 4	T_A = +25°C	-	12	pF
		VDD = Open, f = 1MHz	1, 2, 4	T_A = +25°C	-	12	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz	1, 2, 4	T_A = +25°C	-	12	pF
		VDD = Open, f = 1MHz	1, 2, 4	T_A = +25°C	-	12	pF
Write Enable to Output in High Z	TWLQZ	VDD = 4.5V and 5.5V	1	$-55°C \leq T_A \leq +125°C$	-	10	ns

Absolute Maximum Ratings

Supply Voltage	+7.0V
Input, Output or I/O Voltage	GND-0.3V to VDD+0.3V
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+175°C
Lead Temperature (Soldering 10s)	+300°C
Typical Derating Factor	3mA/MHz Increase in IDDOP
ESD Classification	Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
28 Lead SBDIP Package	45°C/W	8.0°C/W
28/36 Lead Ceramic Flatpack Package	53.4°C/W	7.4°C/W

Maximum Package Power Dissipation at +125°C Ambient

28 Lead SBDIP Package	1.11W
28/36 Lead Ceramic Flatpack Package	0.94W

If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:

28 Lead SBDIP Package	22.2mW/C
28/36 Lead Ceramic Flatpack Package	18.7mW/C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range (VDD)	+4.5V to +5.5V
Operating Temperature Range (T_A)	-55°C to +125°C
Input Low Voltage (VIL)	0V to +0.2VDD
Input High Voltage (VIH)	0.8VDD to VDD
Data Retention Supply Voltage	2.0V
Input Rise and Fall Time	40ns Max.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

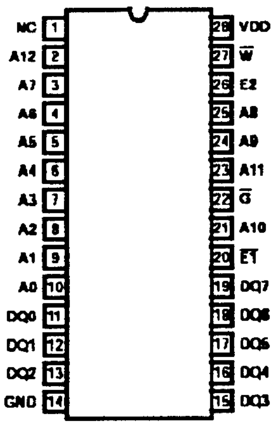
PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
High Level Output Voltage	VOH	VDD = 4.5V, IO = -5mA VI = VDD or GND	1, 2, 3	-55°C, +25°C, +85°C, +125°C	VDD-0.4	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 8.0mA VI = VDD or GND	1, 2, 3	-55°C, +25°C, +85°C, +125°C	-	0.4	V
High Impedance Output Leakage Current	IOZL or IOZH	VDD = 5.5V, VO = GND or VDD, VI = VDD or GND $\overline{E1}$ = VDD, E2 = 0V	1, 3	-55°C, +25°C	-10	10	µA
			2	+85°C	-30	30	µA
			2	+125°C	-60	60	µA
Input Leakage Current	IIH or IIL	VDD = 5.5V, VI = VDD or GND	1, 2, 3	-55°C, +25°C, +85°C, +125°C	-1.0	1.0	µA
Standby Supply Current	IDDSB (Note 3)	VDD = 5.5V, IO = 0mA, VI = VDD or GND $\overline{E1}$ = VDD, E2 = 0V	1, 3	-55°C, +25°C	-	500	µA
			2	+85°C	-	4	mA
			2	+125°C	-	10	mA
Enable Supply Current	IDDEN	VDD = 5.5V, IO = 0mA, VI = VDD or GND $\overline{E1}$ = 0.0V, E2 = VDD	3	-55°C	-	77	mA
			1	+25°C	-	73	mA
			2	+85°C, +125°C	-	64	mA
Operating Supply Current (Note 2)	IDDOP	VDD = 5.5V, IO = 0mA, VI = VDD or GND, E2 = VDD, $\overline{E1}$ = 0V, f = 2MHz	3	-55°C	-	100	mA
			1	+25°C	-	86	mA
			2	+85°C, +125°C	-	75	mA
Data Retention Supply Current	IDDDR	VDD = 2.0V, IO = 0mA, VI = VDD or GND $\overline{E1}$ = VDD, E2 = 0V	1, 3	-55°C, +25°C	-	50	µA
			2	+85°C	-	1	mA
			2	+125°C	-	4	mA
Functional Tests	FT	VDD = 4.5V and 5.5V VI = VDD or GND, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +85°C, +125°C	-	-	-
Noise Immunity Functional Test	FN	VDD = 4.5, VIL = 0.2 VDD VIH = 0.8 VDD, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +85°C, +125°C	-	-	-

NOTES:

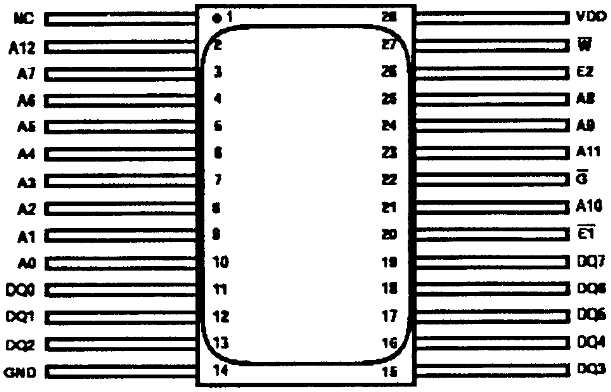
1. All voltages referenced to device GND.
2. Typical IDDOP derating = 3mA/MHz (3mA increase in IDDOP per 1MHz increase in address frequency.)
3. In order for this device to be in low power standby mode. E2 must be disabled (low).

Pinouts

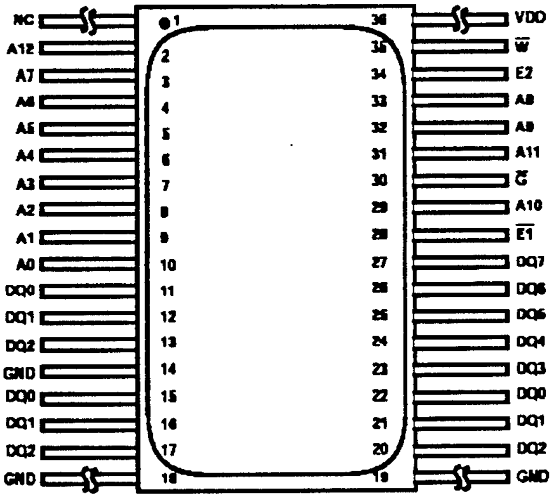
HS1-65647RH 28 LEAD CERAMIC DUAL-IN-LINE
METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T28
TOP VIEW



HS9-65647RH 28 LEAD CERAMIC METAL
SEAL FLATPACK PACKAGE (FLATPACK)
MIL-STD-1835 CDFP3-F28
TOP VIEW



HS9A-65647RH 36 LEAD CERAMIC METAL
SEAL FLATPACK PACKAGE (FLATPACK)
HARRIS OUTLINE K36.A
TOP VIEW



HARRIS
SEMICONDUCTOR

HS-65647RH

Radiation Hardened 8K x 8 SOS CMOS Static RAM

August 1995

Features

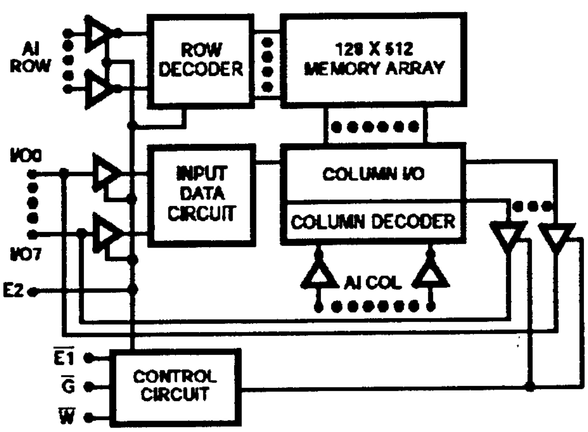
- 1.2 Micron Radiation Hardened SOS CMOS
  - Total Dose 3 x 10^5 RAD (Si)
  - Transient Upset >1 x 10^{11} RAD (Si)/s
  - Single Event Upset < 1 x 10^{-12} Errors/Bit-Day
- Latch-up Free
- LET Threshold >250 MEV/mg/cm2
- Low Standby Supply Current 10mA (Max)
- Low Operating Supply Current 100mA (2MHz)
- Fast Access Time 50ns (Max), 35ns (Typ)
- High Output Drive Capability
- Gated Input Buffers (Gated by E2)
- Six Transistor Memory Cell
- Fully Static Design
- Asynchronous Operation
- CMOS Inputs
- 5V Single Power Supply
- Military Temperature Range -55°C to +125°C
- Industry Standard JEDEC Pinout

Description

The Harris HS-65647RH is a fully asynchronous 8K x 8 radiation hardened static RAM. This RAM is fabricated using the Harris 1.2 micron silicon-on-sapphire CMOS technology. This technology gives exceptional hardness to all types of radiation, including neutron fluence, total ionizing dose, high intensity ionizing dose rates, and cosmic rays.

Low power operation is provided by a fully static design. Low standby power can be achieved without pull-up resistors, due to the gated input buffer design.

Functional Diagram



TRUTH TABLE

$\overline{\text{E1}}$	E2	$\overline{\text{G}}$	$\overline{\text{W}}$	MODE
X	0	X	X	Low Power Standby
1	1	X	X	Disabled
0	1	1	1	Enabled
0	1	0	1	Read
0	1	X	0	Write

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HS1-65647RH-Q	-55°C to +125°C	28 Lead SBDIP
HS1-65647RH-8	-55°C to +125°C	28 Lead SBDIP
HS1-65647RH/Proto	-55°C to +125°C	28 Lead SBDIP
HS1-65647RH/Sample	+25°C	28 Lead SBDIP
HS9-65647RH-Q	-55°C to +125°C	28 Lead Ceramic Flatpack
HS9-65647RH-8	-55°C to +125°C	28 Lead Ceramic Flatpack
HS9-65647RH/Proto	-55°C to +125°C	28 Lead Ceramic Flatpack
HS9-65647RH/Sample	+25°C	28 Lead Ceramic Flatpack
HS9A-65647RH-Q	-55°C to +125°C	36 Lead Ceramic Flatpack

DESIGN INFORMATION (Continued)

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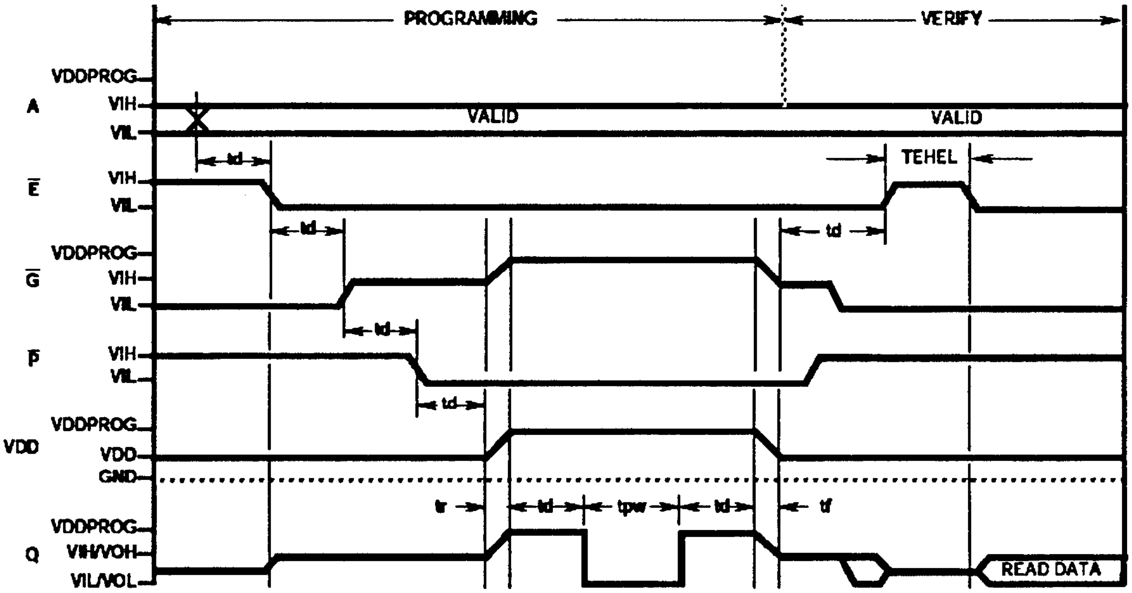
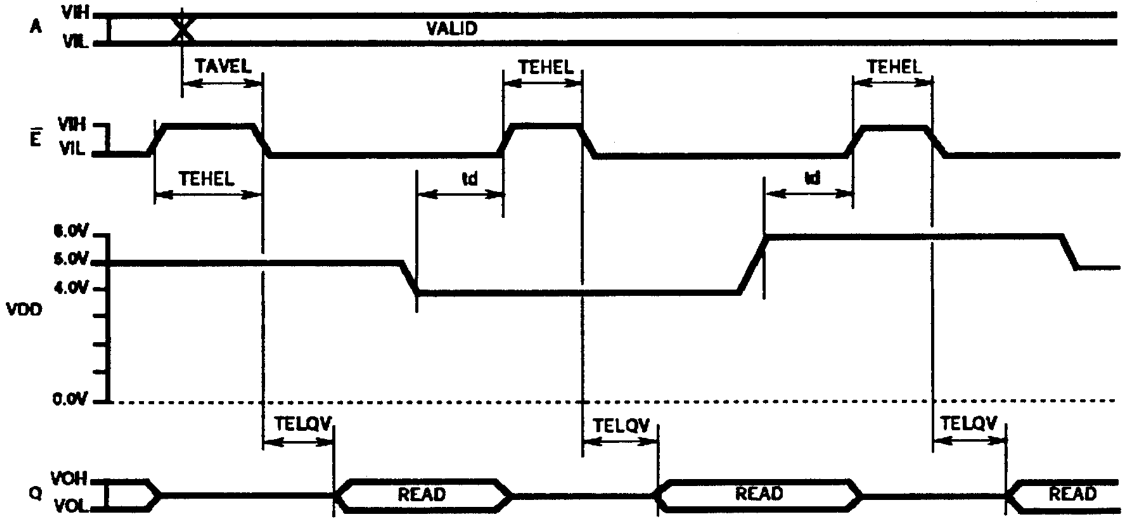
HS-6664RH PROGRAMMING CYCLE



HS-6664RH POST PROGRAMMING VERIFY CYCLE



DESIGN INFORMATION (Continued)

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Background Information Programming

The HS-6664 CMOS PROM is manufactured with all bits containing a logical zero (output low). Any bit can be programmed selectively to a logical one (output high) state by following the procedure shown below. To accomplish this, a programmer can be built that meets the specifications shown, or use of an approved commercial programmer is recommended.

Programming Sequence of Events

1. Apply a voltage of VDD1 to VDD of the PROM.
2. Read all fuse locations to verify that the PROM is blank (output low).
3. Place the PROM in the initial state for programming:
   $\overline{E}$ = VIH, $\overline{P}$ = VIH, $\overline{G}$ = VIL.
4. Apply the correct binary address for the word to be programmed. No inputs should be left open circuit.
5. After a delay of td, apply voltage of VIL to $\overline{E}$ (pin 20) to access the addressed word.
6. The address may be held through the cycle, but must be held valid at least for a time equal to td after the falling edge of $\overline{E}$. None of the inputs should be allowed to float to an invalid logic level.
7. After a delay of td, disable the outputs by applying a voltage of VIH to $\overline{G}$ (pin 22).
8. After a delay of td, apply voltage of VIL to $\overline{P}$ (pin 27).
9. After delay of td, raise VDD (pin 28) to VDDPROG with a rise time of tr. All outputs at VIH should track VDD within VDD-2.0V to VDD+0.3V. This could be accomplished by pulling outputs at VIH to VDD through pull-up resistors of value Rn.
10. After a delay of td, pull the output which corresponds to the bit to be programmed to VIL. Only one bit should be programmed at a time.
11. After a delay of tpw, allow the output to be pulled to VIH through pull-up resistor Rn.
12. After a delay of td, reduce VDD (pin 28) to VDD1 with a fall time of tf. All outputs at VIH should track VDD with VDD-2.0V to VDD+0.3V. This could be accomplished by pulling outputs at VIH to VDD through pull-up resistors of value Rn.
13. Apply a voltage of VIH to $\overline{P}$ (pin 27).
14. After a delay of td, apply a voltage of VIL to $\overline{G}$ (pin 22).
15. After a delay of td, examine the outputs for correct data. If any location verifies incorrectly, it should be considered a programming reject.
16. Repeat steps 3 through 15 for all other bits to be programmed in the PROM.

Post-Programming Verification

17. Place the PROM in the post-programming verification mode:
    $\overline{E}$ = VIH, $\overline{G}$ = VIL, $\overline{P}$ = VIH, VDD (pin 28) = VDD1.
18. Apply the correct binary address of the word to be verified to the PROM.
19. After a delay of td, apply a voltage of VIL to $\overline{E}$ (pin 20).
20. After a delay of td, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.
21. Repeat steps 17 through 20 for all possible programming locations.

Post-Programming Read

22. Apply a voltage of VDD2 = 4.0V to VDD (pin 28).
23. After a delay of td, apply a voltage of VIH to $\overline{E}$ (pin 20).
24. Apply the correct binary address of the word to be read.
25. After a delay of TAVEL, apply a voltage of VIL to $\overline{E}$ (pin 20).
26. After a delay of TELQV, examine the outputs for correct data. If any location fails to verify correctly, the PROM should be considered a programming reject.
27. Repeat steps 23 through 26 for all address locations.
28. Apply a voltage of VDD2 = 6.0V to VDD (pin 28).
29. Repeat steps 23 through 26 for all address locations.

HS-6664RH

DESIGN INFORMATION

September 1995

8K x 8 CMOS PROM

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Background Information HS-6664RH Programming

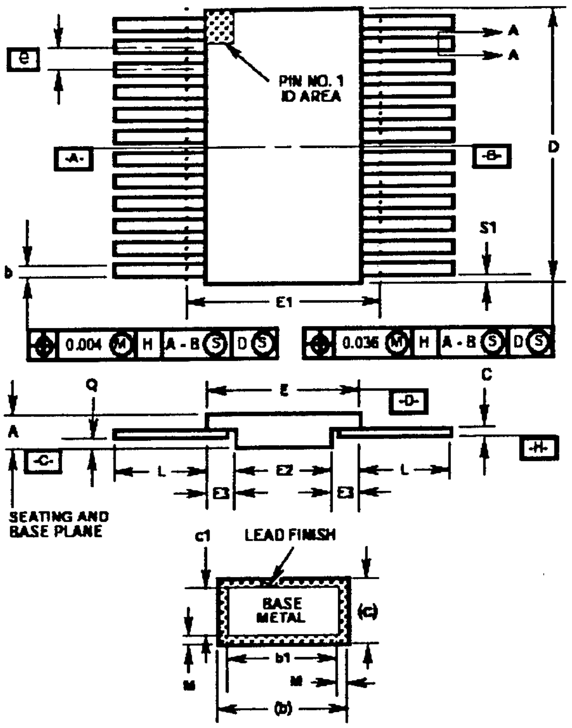
PROGRAMMING SPECIFICATIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input "0"	VIL	0.0	0.2	0.8	V	
Voltage "1"	VIH	VDD-2	VDD	VDD+0.3	V	6
Programming VDD	VDDPROG	9.0	9.0	9.0	V	2
Operating VDD	VDD1	4.5	5.5	5.5	V	
Special Verify	VDD2	4.0	-	6.0	V	3
Delay Time	td	1.0	1.0	-	µs	
Rise Time	tr	1.0	10.0	10.0	µs	
Fall Time	tf	1.0	10.0	10.0	µs	
Chip Enable Pulse Width	TEHEL	20	-	-	ns	
Address Valid to Chip Enable Low Time	TAVEL	0	-	-	ns	
Chip Enable Low to Output Valid Time	TELQV	-	-	60	ns	
Programming Pulse Width	tpw	90	100	110	µs	4
Input Leakage at VDD = VDDPROG	tIP	-10	+1.0	10	µA	
Data Output Current at VDD = VDDPROG	IOP	-	-5.0	-10	mA	
Output Pull-Up Resistor	Rn	5	10	15	kΩ	5
Ambient Temperature	T_A	-	25	-	°C	

NOTES:

1. All inputs must track VDD (pin 28) within these limits.
2. VDDPROG must be capable of supplying 500mA. VDDPROG Power Supply tolerance ±3% (Max.)
3. See Steps 22 through 29 of the Programming Algorithm.
4. See Step 11 of the Programming Algorithm.
5. All outputs should be pulled up to VDD through a resistor of value Rn.
6. Except during programming (See Programming Cycle Waveforms).

Packaging (Continued)



SECTION A-A

K28.A MIL-STD-1835 CDFP3-F28 (F-11A, CONFIGURATION B)
28 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

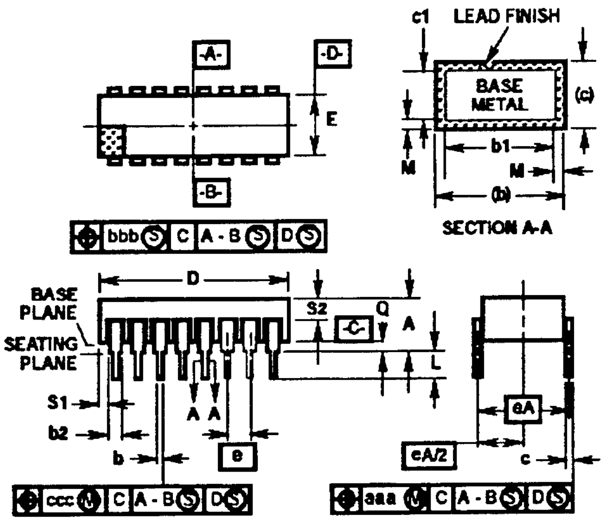
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.740	-	18.80	3
E	0.460	0.520	11.68	13.21	-
E1	-	0.550	-	13.97	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	28		28		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Packaging



D28.6 MIL-STD-1835 CDIP2-T28 (D-10, CONFIGURATION C)
28 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	-
E	0.500	0.610	12.70	15.49	-
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	28		28		8

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Metallization Topology

DIE DIMENSIONS:
271 x 307 x 19 ±1mils

METALLIZATION:
M1: 6kÅ ±1kÅ Si/Al/Cu
2kÅ ±500Å TiW
M2: 10kÅ ± 2kÅSi/Al/Cu

GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
2×10^5 A/cm^2

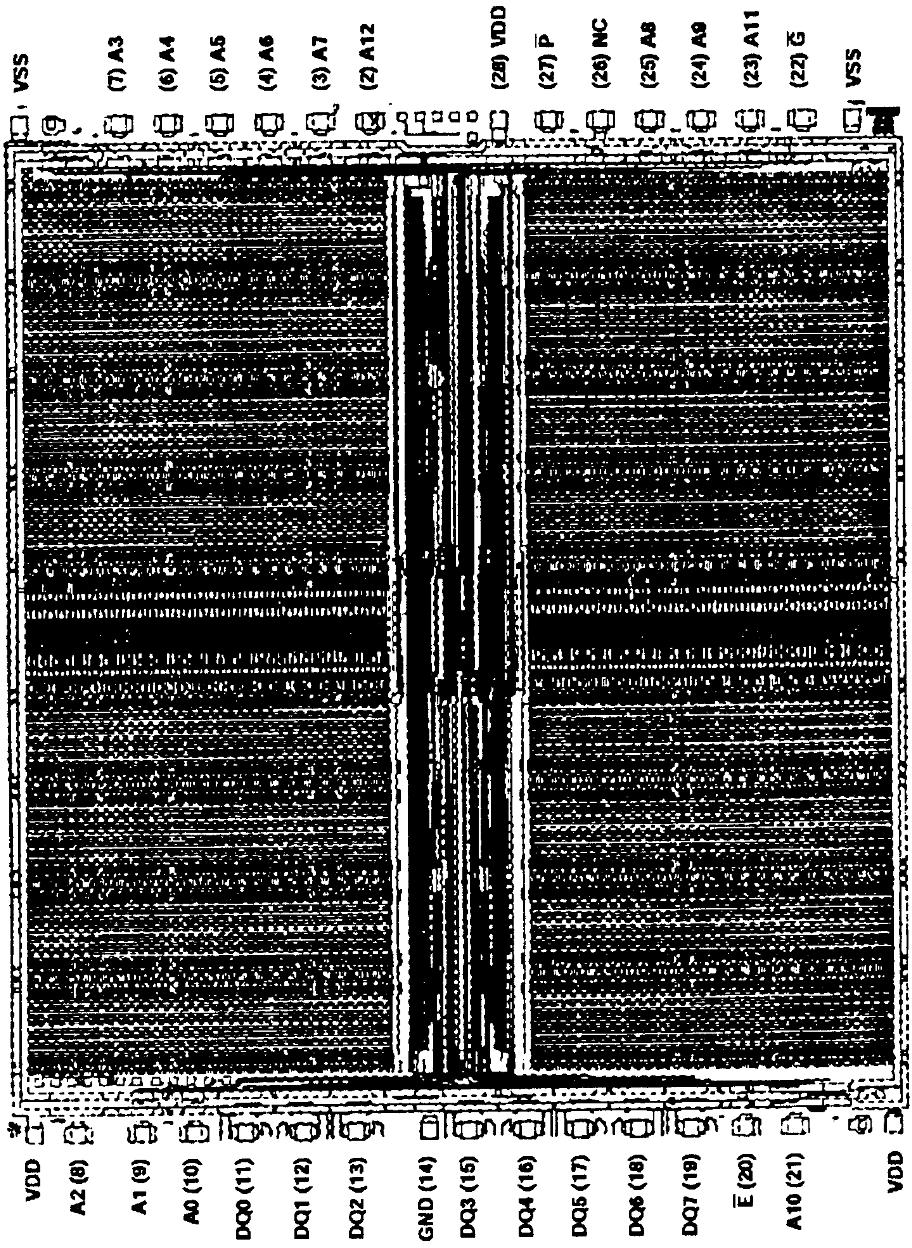
SUBSTRATE POTENTIAL: VDD

TRANSISTOR COUNT: 110, 874

GATE COUNT: 27, 719 (Based on 2-Input NAND)

Metallization Mask Layout

HS-6664RH



Harris - Space Level (-Q) Product Flow (Note 1)

SEM - Traceable to Diffusion Method 2018

Wafer Lot Acceptance Method 5007

Internal Visual Inspection Method 2010, Condition A

Gamma Radiation Assurance Tests Method 1019

Nondestructive Bond Pull Method 2023

Customer Pre-Cap Visual Inspection (Note 2)

Temperature Cycling Method 1010, Condition C

Constant Acceleration Method 2001, Condition E Min, Y1

Particle Impact Noise Detection Method 2020, Condition A

Electrical Tests (Harris' Option)

Serialization

X-Ray Inspection Method 2012

Electrical Tests - Subgroup 1; Read and Record (T0)

Static Burn-In Method 1015, Condition B, 72 Hrs, +125°C Min.

Interim 1 Electrical Tests - Subgroup 1; Read and Record (T1)

Burn-In Delta Calculation (T0 -T1)

PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ

Dynamic Burn-In Method 1015, Condition D, 240 Hrs, +125°C (Note 3)

Interim 2 Electrical Tests - Subgroup 1; Read and Record (T2)

Alternate Group A - Subgroups 1, 7, 9; Method 5005; Para 3.5.1.1

Burn-In Delta Calculation (T0 - T2)

PDA Calculation 3% Subgroup 7
5% Subgroups 1, 7, Δ

Electrical Tests - Subgroup 3; Read and Record

Alternate Group A - Subgroups 3, 8B, 11; Method 5005; Para 3.5.1.1

Marking

Electrical Tests - Subgroup 2; Read and Record

Alternate Group A - Subgroups 2, 8A, 10; Method 5005; Para 3.5.1.1

Gross Leak Tests Method 1014, 100%

Fine Leak Tests Method 1014, 100%

Customer Source Inspection (Note 2)

Group B Inspection Method 5005 (Note 2)
  End-Point Electrical Parameters: B-5 - Subgroups 1, 2, 3, 7, 8A, 8B, 9, 10, 11; B-6 - Subgroups 1, 7, 9

Group D Inspection Method 5005 (Notes 2, 4)
  End-Point Electrical Parameters: Subgroups 1, 7, 9

External Visual Inspection Method 2009

Data Package Generation (Note 4)

NOTES:

1. The notes of Method 5004, Table 1 shall apply; Unless Otherwise Specified.
2. These steps are optional, and should be listed on the individual purchase order(s), when required.
3. Harris reserves the right of performing burn-in time temperature regression as defined by Table 1 of Method 1015.
4. Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Shippable Serial Number List
   Radiation Testing Certificate of Conformance
   Wafer Lot Acceptance Report (including SEM Report)
   X-Ray Report and Film
   Test Variables Data

Harris -8 Product Flow

Internal Visual Inspection Method 2010 Condition B Alternate

Gamma Radiation Assurance Tests Method 1019

Customer Pre-Cap Visual Inspection (Note 1)

Temperature Cycling Method 1010, Condition C

Fine and Gross Leak Tests Method 1014

Constant Acceleration Method 2001 Y1 30KG

Initial Electrical Tests

Dynamic Burn-In Method 1015, Condition D, 160 Hrs, +125°C

+25°C Electrical Tests - Subgroups 1, 7, 9

PDA Calculation 5% Subgroups 1, 7

Electrical Tests +125°C, -55°C

Group A Inspection Method 5005. 5% PDA (Note 3)

Brand

Customer Source Inspection (Note 1)

Group B Inspection Method 5005 (Notes 1, 2)

Group C Inspection Method 5005 (Notes 1, 2)

Group D Inspection Method 5005 (Notes 1, 2)

External Visual Inspection Method 2009

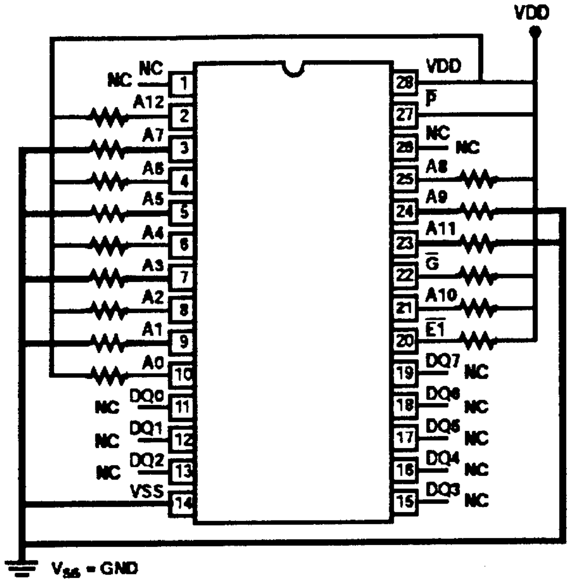
Data Package Generation (Note 4)

NOTES:

1. These steps are optional, and must be negotiated as part of order.
2. Group B, C and D data package contains Attributes Data.
3. Harris reserves the right to perform Alternate Group A. The 5% PDA is still applicable.
4. '-8' Data package contains:
   Assembly Attributes (post seal)
   Test Attributes (includes Group A)
   Radiation Testing Certificate of Conformance
   Certificate of Conformance (as found on shipper)

Burn-In Circuits

HS1-6664RH 28 LEAD (8K x 8 PROM DIP)
HS9-6664RH 28 LEAD (8K x 8 PROM FLATPACK)

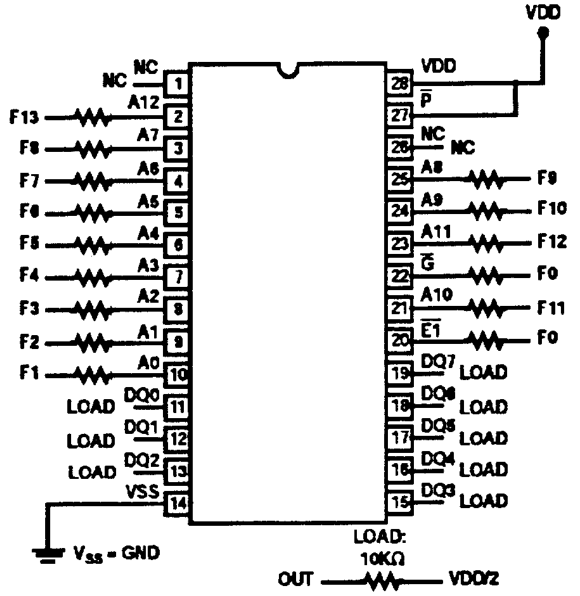


STATIC CONFIGURATION

NOTES:

1. Power Supply: VDD = 5.5V (Min)
2. Resistors = 10kΩ ± 10%

HS1-6664RH 28 LEAD (8K x 8 PROM DIP)
HS9-6664RH 28 LEAD (8K x 8 PROM FLATPACK)



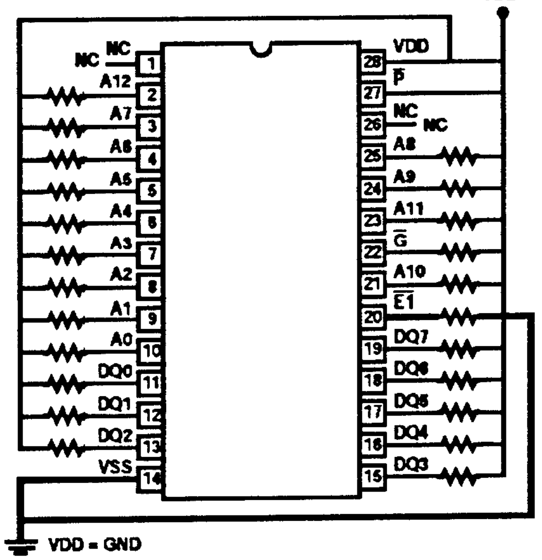
DYNAMIC CONFIGURATION

NOTES:

1. Power Supply: VDD = 5.5V (Min)
2. VIH = VDD to VDD-1.0V
3. VIL = 0.0V to 0.8V
4. Resistors = 10KΩ ± 10%
5. F0 = 100KHz ± 10%, 50% Duty Cycle
6. F1 = F0/2; F2 = F1/2; F3 = F2/2; F4 = F3/2; F5 = F4/2; . . . F13 = F12/2

Irradiation Circuit

HS1-6664RH 28 LEAD (8K x 8 PROM DIP)



NOTES:

1. Power Supply: VDD = 5.5V ±0.5V
2. All Resistors = 47KΩ ± 10%

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	-8 SUBGROUPS
Initial Test		100%/5004	1, 7, 9	1, 7, 9
Interim Test		100%/5004	1, 7, 9	1, 7, 9
PDA 1 and 2		100%/5004	1, 7, Δ	1, 7
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	2, 3, 8A, 8B, 10, 11
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group B (*Optional)	B5	Samples/5005	1, 2, 3, 7, 8A, 8B	N/A
	Others	Samples/5005	1, 7,9	N/A
Group C (Optional)		Samples/5005	N/A	1, 7, 9
Group D (Optional)		Samples/5005	1, 7, 9	1, 7, 9
Group E, Subgroup 2 (Note 1)		Samples/5005	1, 7, 9	1, 7, 9

NOTE:

1. Harris may exercise its option to perform to a small lot sampling plan of 5 units per lot.

Timing Waveform

READ CYCLE

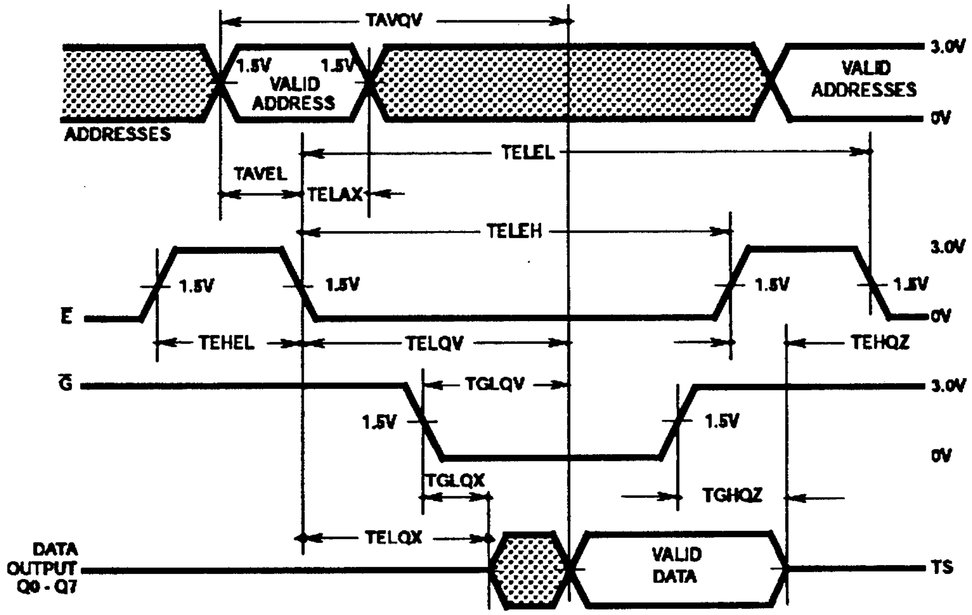


TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Guaranteed and 100% Tested.

PARAMETER	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Chip Enable Low Width	TELEH	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	60	-	ns
Chip Enable High Width	TEHEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	20	-	ns
Read Cycle Time	TELEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	80	-	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume transition time ≤ 5ns; input levels = 0.0V to 3.0V; timing reference levels = 1.5V; output load = 1 TTL equivalent load and CL ≥ 50pF.
3. All tests performed with $\overline{P}$ hardwired to VDD.
4. Address Access Time (TAVQV) = TELQV + TAVEL = 65ns (maximum).

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS, AC AND DC

PARAMETER	SYMBOL	(NOTE 2) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	1, 3	$T_A = +25^{\circ}C$	-	15	pF
I/O Capacitance	CI/O	VDD = Open, f = 1MHz	1, 3	$T_A = +25^{\circ}C$	-	12	pF
Chip Enable Time	TELQX	VDD = 4.5V and 5.5V	3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	5	-	ns
Output Enable Time	TGLQX	VDD = 4.5V and 5.5V	3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	5	-	ns
Chip Disable Time	TEHQZ	VDD = 4.5V and 5.5V	3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-	15	ns
Output Disable Time	TGHQZ	VDD = 4.5V and 5.5V	3	$-55^{\circ}C \leq T_A \leq +125^{\circ}C$	-	15	ns

NOTES:

1. All measurements referenced to device GND.
2. All tests performed with $\overline{P}$ hardwired to VDD.
3. The parameters listed are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after design or process changes which would affect these characteristics.

TABLE 4. POST 100K RAD AC AND DC ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: All AC and DC parameters are tested at the +25°C pre-irradiation limits.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Standby Supply Current	IDDSB	±50µA
Input Leakage Current	IOZ	±1µA
	II	±100nA
Output Low Voltage	VOL	±60mV
Output High Voltage	VOH	±400mV

Absolute Maximum Ratings

Supply Voltage (All Voltages Reference to Device GND). . . . . +7.0V
Input or Output Voltage
Applied for All Grades. . . . . GND-0.3V to VDD+0.3V
Storage Temperature Range . . . . -65°C to +150°C
Junction Temperature. . . . . +175°C
Lead Temperature (Soldering 10s). . . . . +300°C
ESD Classification . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
Braze Seal DIP Package	40.0°C/W	4.0°C/W
Braze Seal Flatpack Package	53.4°C/W	6.0°C/W

Maximum Package Power Dissipation at +125°C
Braze Seal DIP Package. 1.75W
Braze Seal Flatpack Package 936mW
Gate Count . . . . 26,817 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Supply Voltage Range (VDD) . . . . +4.5V to +5.5V
Operating Temperature Range (T_A) . . . . -55°C to +125°C
Input Low Voltage (VIL). . . . . 0V to +0.8V
Input High Voltage (VIH) . . . . +2.4V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
High Level Output Voltage	VOH1	VDD = 4.5V, IO = -2.0mA	1, 2, 3	$-55°C \le T_A \le +125°C$	3.5	-	V
Output High Voltage	VOH2	VDD = 4.5V, IO = 100μA	3	$-55°C \le T_A \le +125°C$	VDD -0.3V	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, IO = 4.8mA	1, 2, 3	$-55°C \le T_A \le +125°C$	-	0.4	V
High Impedance Output Leakage Current	IOZ	VDD = 5.5V, $\overline{G}$ = 5.5V, VI/O = GND or VDD	1, 2, 3	$-55°C \le T_A \le +125°C$	-10.0	10.0	μA
Input Leakage Current	II	VDD = 5.5V, VI = GND or VDD, $\overline{P}$ Not Tested	1, 2, 3	$-55°C \le T_A \le +125°C$	-1.0	1.0	μA
Standby Supply Current	IDDSB	VDD = 5.5V, IO = 0mA, VI = VDD or GND	1, 2, 3	$-55°C \le T_A \le +125°C$	-	500	μA
Operating Supply Current	IDDOP	VDD = 5.5V, $\overline{G}$ = VDD, (Note 3), f = 1MHz, IO = 0mA, VI = VDD or GND	1, 2, 3	$-55°C \le T_A \le +125°C$	-	15	mA
Functional Test	FT	VDD = 4.5V (Note 4)	7, 8A, 8B	$-55°C \le T_A \le +125°C$	-	-	-

NOTES:

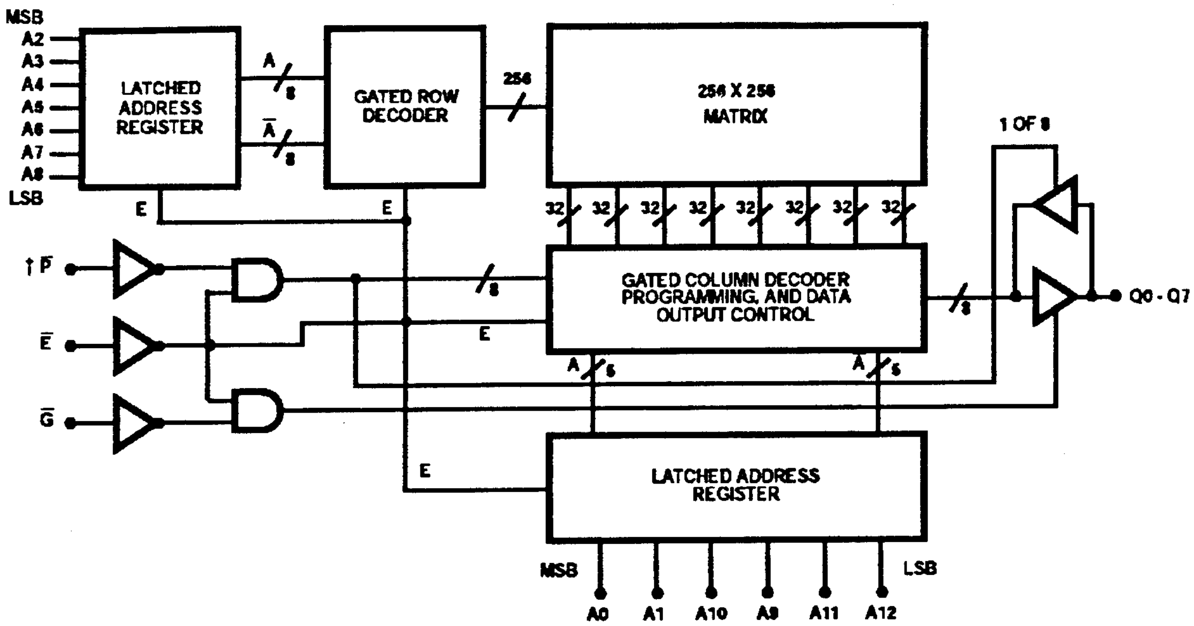
1. All voltages referenced to device GND.
2. All tests performed with $\overline{P}$ hardwired to VDD.
3. Typical derating = 15mA/MHz increase in IDDOP.
4. Tested as follows: f = 1MHz, VIH = 2.4V, VIL = 0.45V, IOH = -1mA, IOL = +1mA, VOH ≥ 1.5V, VOL ≤ 1.5V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Guaranteed and 100% Tested.

PARAMETER	SYMBOL	(NOTES 1, 2, 3) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Enable Access Time	TGLQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	20	ns
Chip Enable Access Time	TELQV	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	-	60	ns
Address Setup Time	TAVEL	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	5	-	ns
Address Hold Time	TELAX	VDD = 4.5V and 5.5V	9, 10, 11	$-55°C \le T_A \le +125°C$	12	-	ns

Functional Diagram



† P must be hardwired at all times to VDD, except during programming.

TRUTH TABLE

$\overline{E}$	$\overline{G}$	MODE
0	0	Enabled
0	1	Output Disabled
1	X	Disabled

HARRIS
SEMICONDUCTOR

HS-6664RH

Radiation Hardened 8K x 8 CMOS PROM

September 1995

Features

- 1.2 Micron Radiation Hardened Bulk CMOS
- Total Dose 3 x 10^5 RAD (Si)
- Transient Output Upset >5 x 10^8 RAD (Si)/s
- LET >100 MEV-cm^2/mg
- Fast Access Time - 35ns (Typical)
- Single 5V Power Supply
- Single Pulse 10V Field Programmable
- Synchronous Operation
- On-Chip Address Latches
- Three-State Outputs
- NiCr Fuses
- Low Standby Current <500µA (Pre-Rad)
- Low Operating Current <15mA/MHz
- Military Temperature Range -55°C to +125°C

Description

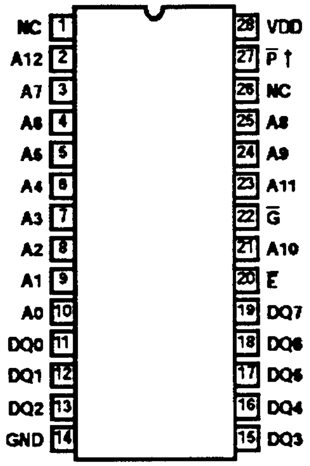
The Harris HS-6664RH is a radiation hardened 64K CMOS PROM, organized in an 8K word by 8-bit format. The chip is manufactured using a radiation hardened CMOS process, and utilizes synchronous circuit design techniques to achieve high speed performance with very low power dissipation.

On-chip address latches are provided, allowing easy interfacing with microprocessors that use a multiplexed address/data bus structure. The output enable control ($\overline{G}$) simplifies system interfacing by allowing output data bus control in addition to the chip enable control ($\overline{E}$). All bits are manufactured storing a logical "0" and can be selectively programmed for a logical "1" at any bit location.

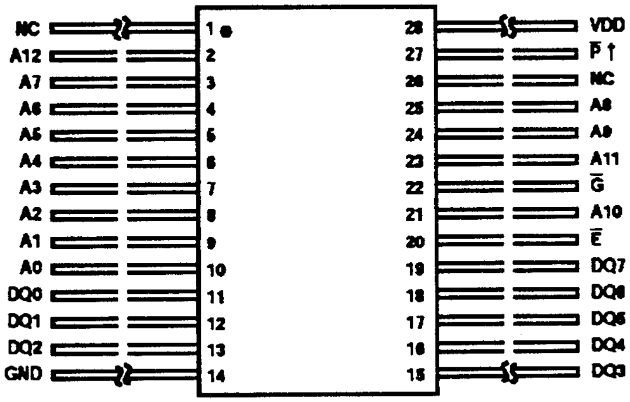
Applications for the HS-6664RH CMOS PROM include low power microprocessor based instrumentation and communications systems, remote data acquisition and processing systems, and processor control storage.

Pinouts

28 LEAD CERAMIC SBDIP
CASE OUTLINE D28.6 MIL-STD-1835, CDIP2-T28
TOP VIEW



28 LEAD FLATPACK
CASE OUTLINE K28.A MIL-STD-1835, CDFP3-F28
TOP VIEW



† P must be hardwired at all times to VDD, except during programming.

ORDERING INFORMATION

UT22VP10: Prototypes and Military Temperature Range

UT 22VP10 *-** * * *

Lead Finish: 1
(A) = Hot solder dipped
(C) = Gold
(X) = Factory option (gold or solder) 2

Screening:
(T) = Military temperature range flow 3
(P) = Prototype flow 4

Package Type:
(P) = 24-lead ceramic side-brazed DIP (0.300" body)
(U) = 24-lead ceramic bottom-brazed dual-in-line flatpack (0.050" lead pitch)
(W) = 28-lead ceramic top-brazed quad-flatpack (0.050" lead pitch)

Device Type Modifier/Speed:
(C-25) = CMOS I/O; 25ns propagation delay
(T-25) = TTL I/O; 25ns propagation delay

Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Military temperature range flow per *UTMC Manufacturing Flows Technical Description*. Devices have 48 hours of burn-in and are tested at -55°C, room temperature, and 125°C. Radiation characteristics are neither tested nor guaranteed and may not be specified.
4. Prototype flow per *UTMC Manufacturing Flows Technical Description*. Devices have prototype assembly and are tested at 25°C only. Radiation characteristics are neither tested nor guaranteed and may not be specified. Lead finish is at UTMC's option and an "X" must be specified when ordering.

UT22VP10: QML Class Q & Class V

5962 - 94754 ** * * *

Lead Finish: 1
(A) = Hot solder dipped
(C) = Gold
(X) = Factory option (gold or solder) 2

Case Outline:
(L) = 24-lead ceramic side-brazed DIP (0.300" body)
(X) = 24-lead ceramic bottom-brazed dual-in-line flatpack (0.050" lead pitch)
(Y) = 28-lead ceramic top-brazed quad-flatpack (0.050" lead pitch)

Class Designator:
(V) = Class V, QML qualified to MIL-I-38535
(Q) = CLASS Q, QML qualified to MIL-I-38535

Device Type/Speed:
(01) = CMOS I/O: 25ns propagation delay
(02) = TTL I/O2; 5ns propagation delay

Drawing Number: No options

Total Dose:
(H) = 1E6 rads(Si) per 5962-94754 drawing
(R) = 1E5 rads(Si) per 5962-94754 drawing

Federal Stock Class Designator: No options

Notes:
1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).

UTMC Main Office
1575 Garden of the Gods Road
Colorado Springs, CO 80907-3486
800-722-1575

Melbourne Sales Office
1901 S. Harbor City Blvd., Suite 802
Melbourne, FL 32901
407-951-4164

Baltimore Sales Office
9881 Broken Land Parkway, Suite 300
Columbia, MD 21046
410-312-5734

South LA Sales Office
101 Columbia Street, Suite 130
Aliso Viejo, CA 92656
714-362-2260

Boston Sales Office
140 Wood Road, Suite 200
Braintree, MA 02184
617-356-5600

North LA Sales Office
77 Fulton Lane, Suite 3
Camarillo, CA 93030
805-445-6665

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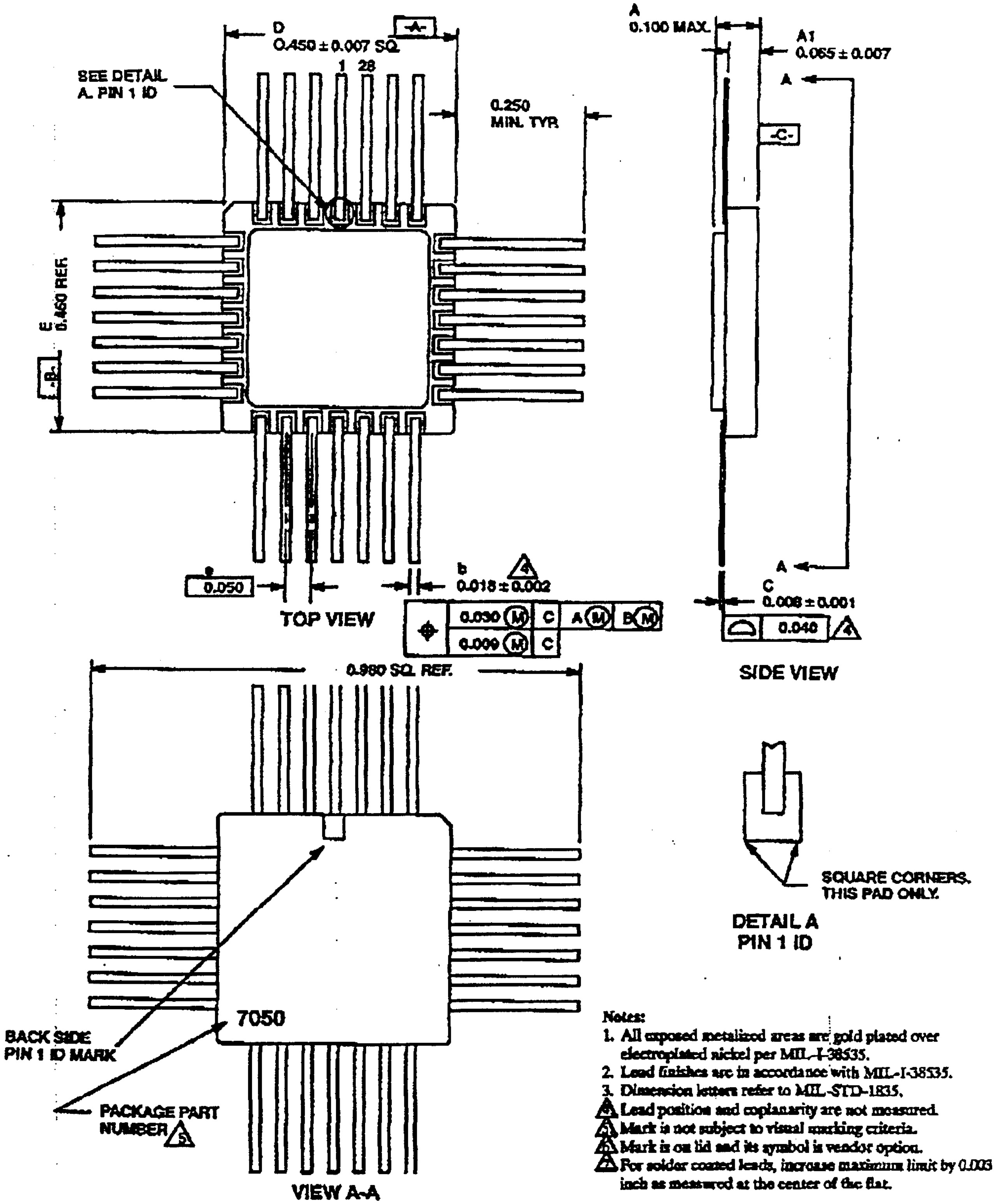
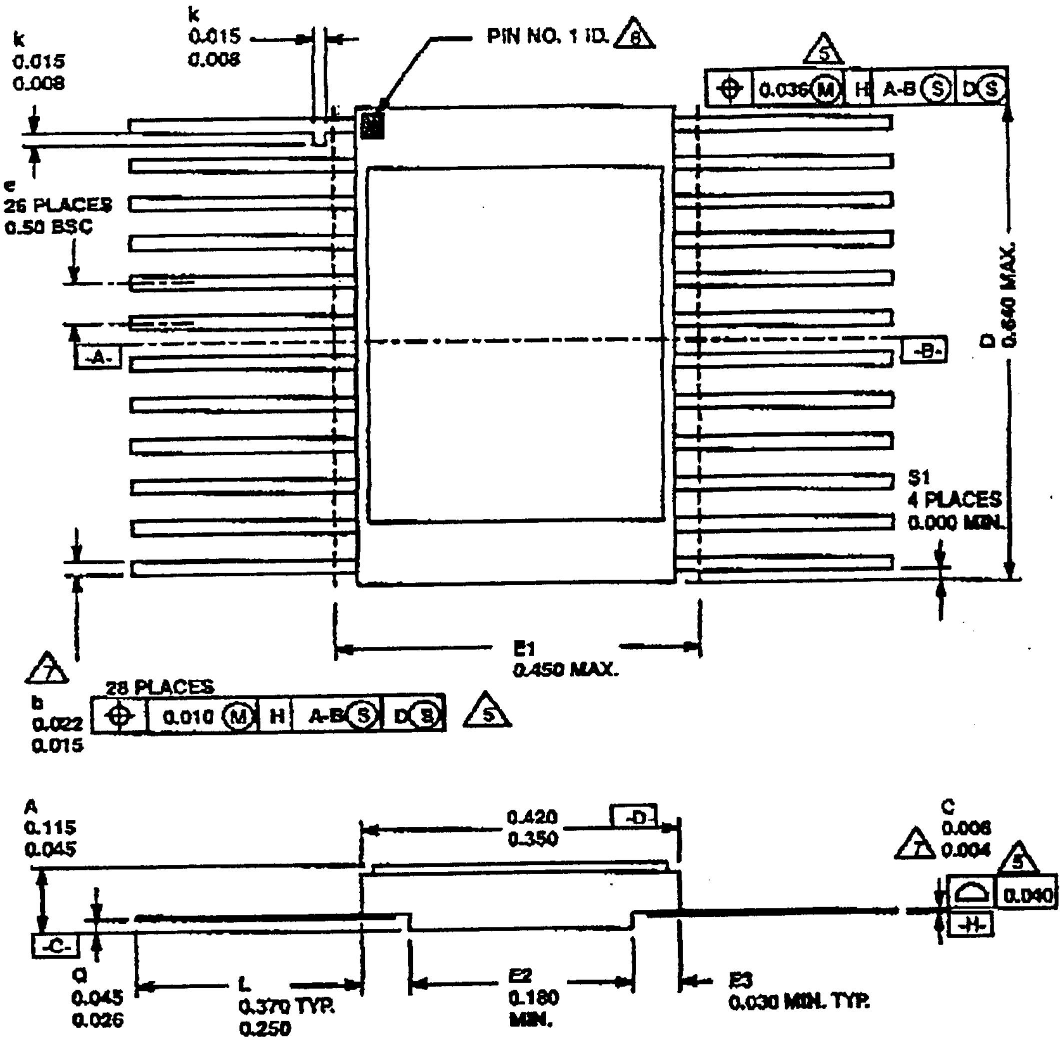
TECHNOLOGIES
MICROELECTRONICS
CENTER



Notes:

1. All exposed metalized areas are gold plated over electroplated nickel per MIL-I-38535.
2. Lead finishes are in accordance with MIL-I-38535.
3. Dimension letters refer to MIL-STD-1835.
4. Lead position and coplanarity are not measured.
5. Mark is not subject to visual marking criteria.
6. Mark is on lid and its symbol is vendor option.
7. For solder coated leads, increase maximum limit by 0.003 inch as measured at the center of the flat.

Figure 9. 28-Lead Quad-Flatpack (.45 x .45)



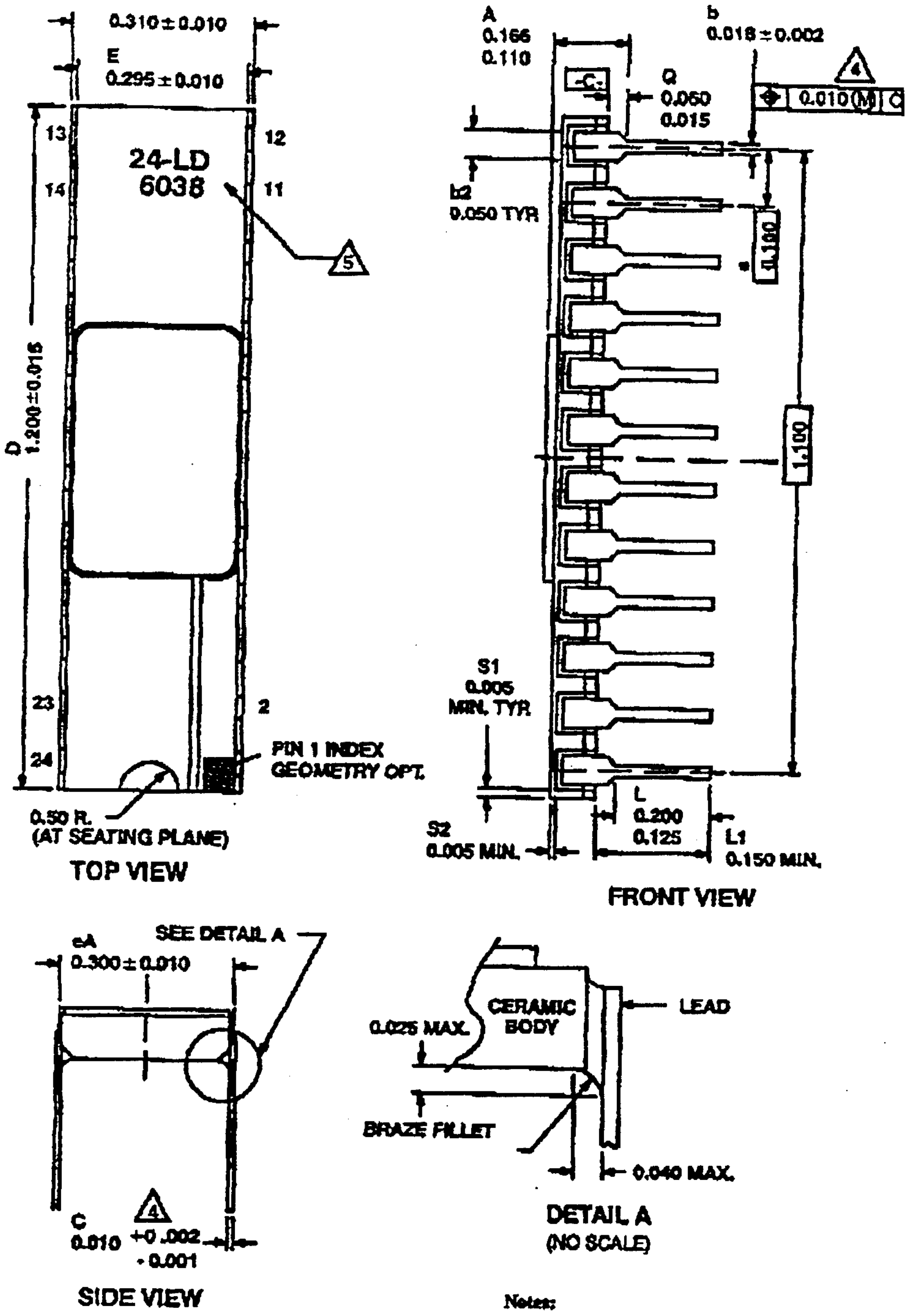
Notes:
1. All exposed metalized areas are gold plated over electroplated nickel per MIL-I-38535.
2. The lid is electrically connected to V_{SS}.
3. Lead finishes are in accordance with MIL-I-38535.
4. Dimension letters refer to MIL-STD-1835.

△5 Lead position and coplanarity are not measured.

△6 ID mark symbol is vendor option.

△7 For solder coated leads, increase maximum limit by 0.003 inch as measured at the center of the flat.

Figure 8. 24-Lead Flatpack (.45 x .64)



Notes:

1. Package material: Opaque ceramic.
2. All exposed metalized areas are finished per MIL-I-38535.
3. Letter designations are for cross-reference to MIL-STD-1835.
4. For solder coated leads, increase maximum limit by 0.003 inch as measured at the center of the flat.
5. Numbering and lettering on the ceramic are not subject to visual marking criteria.

Figure 7. 24-Pin 100-mil Center DIP (0.300 x 1.2)

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. The output state will depend on the programmed pattern. This feature is valuable in simplifying state machine initialization. See figure 6 for a timing diagram. Due to the synchronous operation of the power-up reset and the wide range of ways V_{DD} can rise to its steady state, the following two conditions are required to ensure a valid power-up reset.

- The V_{DD} rise must be monotonic
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

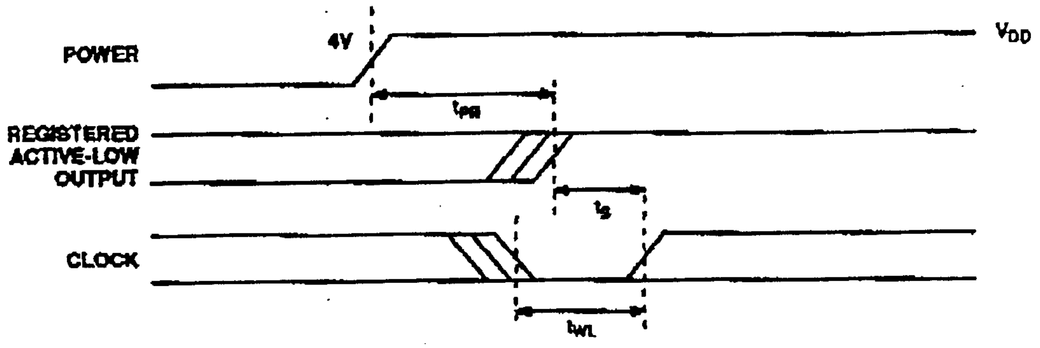


Figure 6. Power-Up Reset Waveform

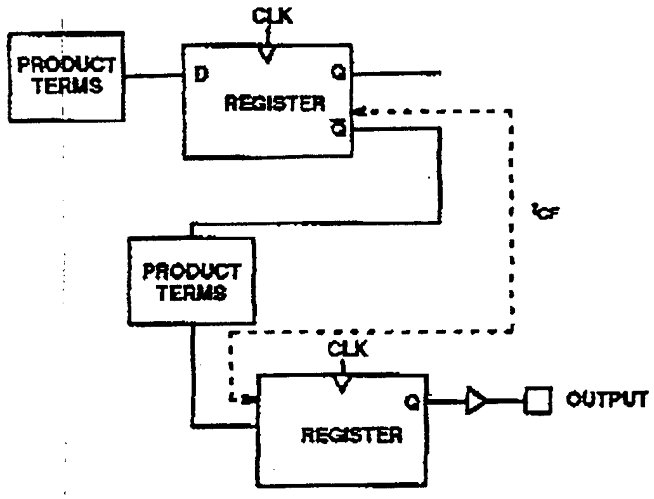
RADIATION HARDNESS

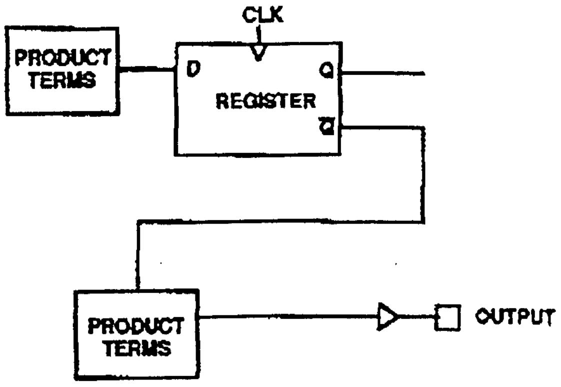
The UT22VP10 RADPAL incorporates special design and layout features which allow operation in high-level radiation environments. UTMC has developed special low-temperature processing techniques designed to enhance the total-dose radiation hardness of both the gate oxide and the field oxide while maintaining the circuit density and reliability. For transient radiation hardness and latchup immunity, UTMC builds all radiation-hardened products on epitaxial wafers using an advanced twin-tub CMOS process.

RADIATION HARDNESS DESIGN SPECIFICATIONS [1]

PARAMETER	CONDITION	MINIMUM	UNIT
Total Dose	+25°C per MIL-STD-883 Method 1019	1.0E6	rads(Si)
LET Threshold	-55°C to +125°C	50	MeV-cm^2/mg
Neutron Fluence	1MeV equivalent	1.0E14	n/cm^2

Note:
1. The RADPAL will not latchup during radiation exposure under recommended operating conditions.



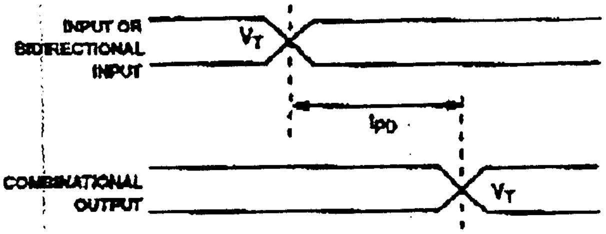


Clock to Combinatorial Output (t_{CO2})

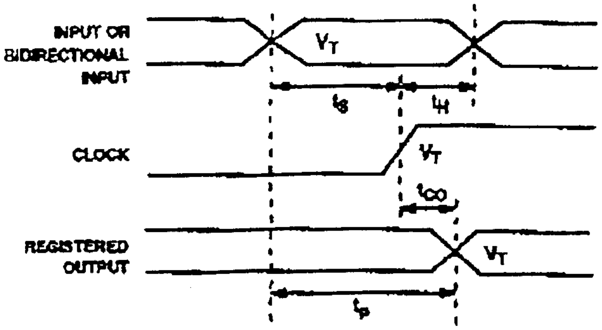
Note:
t_{CF} defined as the propagation delay from $\overline{Q}$ to D register input.

f_{MAX3}: Internal Feedback $\left(\frac{1}{t_{CO} + t_{CF}}\right)$

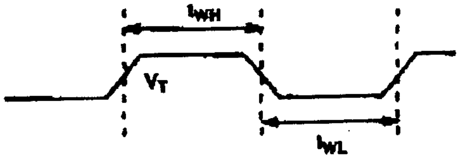
Figure 5. Signal Paths



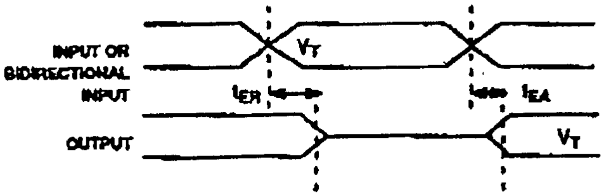
Combinatorial Output



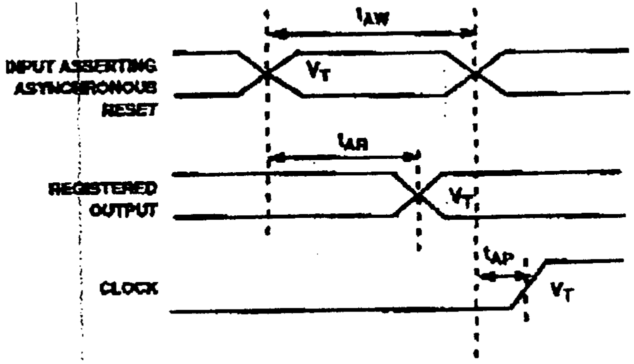
Registered Output



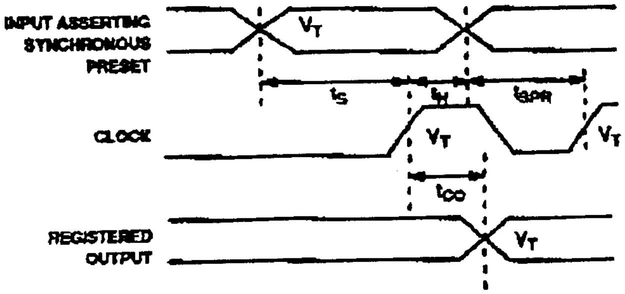
Clock Width



Combinatorial Output
(V_{OH} - 0.5V, V_{OL} + 0.5V)



Asynchronous Reset



Synchronous Preset

Notes:
1. V_T = 1.5V.
2. Input pulse amplitude 0V to 3.0V.
3. Input rise and fall times 3ns maximum.

Figure 4. AC Electrical

AC CHARACTERISTICS READ CYCLE (Post-Radiation) [1,2]
$(V_{DD} = 5.0V \pm 10\%; -55°C < T_C < +125°C)$

SYMBOL	PARAMETER	MINIMUM	MAXIMUM	UNIT
t_{PD}	Input to output propagation delay	–	25	ns
t_{EA}	Input to output enable delay	–	25	ns
t_{ER}	Input to output disable delay	–	25	ns
t_{CO}	Clock to output delay	–	15	ns
t_{CO2}	Clock to combinatorial output delay via internal registered feedback	–	28	ns
t_S	Input or feedback setup time	18	–	ns
t_H	Input or feedback hold time	0	–	ns
t_P	External clock period ($t_{CO} + t_S$)	33	–	ns
$t_{WH, WL}$	Clock width, clock high time, clock low time	14	–	ns
f_{MAX1}	External maximum frequency ($1/(t_{CO} + t_S)$)	30	–	MHz
f_{MAX2}	Data path maximum frequency ($1/(t_{WH} + t_{WL})$)	36	–	MHz
f_{MAX3}	Internal feedback maximum frequency ($1/(t_{CO} + t_{CF})$)	32	–	MHz
t_{CF}	Register clock to feedback input	–	13	ns
t_{AW}	Asynchronous reset width	25	–	ns
t_{AR}	Asynchronous reset recovery time	25	–	ns
t_{AP}	Input to asynchronous reset	–	25	ns
t_{SPR}	Synchronous preset recovery time	25	–	ns
t_{PR}	Power up reset time	1.0	–	µs

Notes:

1. Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019 at 1.0E6 rads(Si).
2. Guaranteed by characterization.

DC ELECTRICAL CHARACTERISTICS [2]

(V_{DD} = 5.0V ± 10%; V_{SS} = 0V [1], -55°C < T_C < +125°C)

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
V_{IL}	Low-level input voltage	TTL	-	.8	V
V_{IH}	High-level input voltage	TTL	2.2	-	V
V_{IL}	Low-level input voltage	CMOS	-	.3*V_{DD}	V
V_{IH}	High-level input voltage	CMOS	.7*V_{DD}	-	V
V_{OL}	Low-level output voltage	I_{OL} = 12.0mA, V_{DD} = 4.5V (TTL)		.4	V
V_{OH}	High-level output voltage	I_{OH} = -12.0mA, V_{DD} = 4.5V (TTL)	2.4	-	V
V_{OL}	Low-level output voltage	I_{OL} = 200µA, V_{DD} = 4.5V (CMOS)	-	V_{SS}+0.05	V
V_{OH}	High-level output voltage	I_{OH} = -200µA, V_{DD} = 4.5V (CMOS)	V_{DD}-0.05	-	V
I_{IN}	Input leakage current	V_{IN} = V_{DD} and V_{SS}	-10	10	µA
I_{OZ}	Three-state output leakage current	V_O = V_{DD} and V_{SS} V_{DD} = 5.5V	-10	10	µA
I_{OS}[3,4]	Short-circuit output current	V_{DD} = 5.5V, V_O = V_{DD} V_{DD} = 5.5V, V_O = 0V	-160	160	mA
C_{IN}[5]	Input capacitance	f=1MHz @0V	-	15	pF
$C_{I/O}$[5]	Bidirectional capacitance	f=1MHz @0V	-	15	pF
I_{CC}	Output three-state, worst-case pattern programmed, f_{MAX1}	V_{DD} = 5.5V	-	120	mA

Notes:
1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si).
3. Duration not to exceed 1 second, one output at a time.
4. Guaranteed, but not tested.
5. Tested for initial qualification only.

Commercial Version (Continued)

DIP ECL-to-TTL AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{TTL} = +4.5V$ to $+5.5V$, $V_{CC} = V_{CCA} = GND$, $C_L = 50$ pF

Symbol	Parameter	$T_C = 0°C$		$T_C = 25°C$		$T_C = 85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.3	5.6	2.4	5.6	2.6	5.9	ns	*Figures 3 & 4*
t_{PLH} t_{PHL}	LE to T_n	3.1	7.2	3.1	7.2	3.3	7.7	ns	*Figures 3 & 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.4 3.8	8.45 9.2	3.7 4.0	8.95 9.2	4.0 4.3	9.7 9.95	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	8.95 7.7	3.3 3.4	8.95 8.7	3.5 4.1	9.2 9.95	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.7 2.8	8.2 7.45	2.8 3.1	8.7 7.95	3.1 4.0	8.95 9.2	ns	*Figures 3 & 6*
t_{set}	E_n to LE	1.1		1.1		1.1		ns	*Figures 3 & 4*
t_{hold}	E_n to LE	2.1		2.1		2.6		ns	*Figures 3 & 4*
$t_{pw}(H)$	Pulse Width LE	4.1		4.1		4.1		ns	*Figures 3 & 4*

SOIC, PCC and Cerpak TTL-to-ECL AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	$T_C = 0°C$		$T_C = 25°C$		$T_C = 85°C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	T_n to E_n (Transparent)	1.1	3.3	1.1	3.4	1.1	3.6	ns ns	*Figures 1 & 2*
t_{PLH} t_{PHL}	LE to E_n	1.7	3.4	1.7	3.5	1.9	3.7	ns ns	*Figures 1 & 2*
t_{PZH}	OE to E_n (Cutoff to High)	1.3	4.0	1.5	4.2	1.7	4.6	ns	*Figures 1 & 2*
t_{PHZ}	OE to E_n (High to Cutoff)	1.5	4.3	1.6	4.3	1.6	4.4	ns	*Figures 1 & 2*
t_{PHZ}	DIR to E_n (High to Cutoff)	1.6	4.1	1.6	4.1	1.7	4.3	ns	*Figures 1 & 2*
t_{set}	T_n to LE	1.0		1.0		1.0		ns	*Figures 1 & 2*
t_{hold}	T_n to LE	1.0		1.0		1.0		ns	*Figures 1 & 2*
$t_{pw}(H)$	Pulse Width LE	2.0		2.0		2.0		ns	*Figures 1 & 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.6	1.6	0.6	1.6	0.6	1.6	ns	*Figures 1 & 2*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		200		200		200	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		650		650		650	ps	PCC Only (Note 1)
t_{ps}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		650		650		650	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} guaranteed by design.

Commercial Version (Continued)

SOIC, PCC and Cerpak ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.3	5.4	2.4	5.4	2.6	5.7	ns	*Figures 3 & 4*
t_{PLH} t_{PHL}	LE to T_n	3.1	7.0	3.1	7.0	3.3	7.5	ns	*Figures 3 & 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.4 3.8	8.25 9.0	3.7 4.0	8.75 9.0	4.0 4.3	9.5 9.75	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	8.75 7.5	3.3 3.4	8.75 8.5	3.5 4.1	9.0 9.75	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.7 2.8	8.0 7.25	2.8 3.1	8.5 7.75	3.1 4.0	8.75 9.0	ns	*Figures 3 & 6*
t_{set}	E_n to LE	1.0		1.0		1.0		ns	*Figures 3 & 4*
t_{hold}	E_n to LE	2.0		2.0		2.6		ns	*Figures 3 & 4*
$t_{pw}(H)$	Pulse Width LE	4.0		4.0		4.0		ns	*Figures 3 & 4*
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		600		600		600	ps	PCC Only (Note 1)
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		850		850		850	ps	PCC Only (Note 1)
t_{OST}	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		1350		1350		1350	ps	PCC Only (Note 1)
t_{ps}	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		950		950		950	ps	PCC Only (Note 1)

Note 1: Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH to LOW (t_{OSHL}), or LOW to HIGH (t_{OSLH}), or in opposite directions both HL and LH (t_{OST}). Parameters t_{OST} and t_{ps} guaranteed by design.

Industrial Version

PCC TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C, V_{TTL} = +4.5V to +5.5V (Note)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	−1085	−870	−1025	−870	mV	V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$ Loading with 50Ω to −2V
V_{OL}	Output LOW Voltage	−1830	−1575	−1830	−1620	mV	
	Cutoff Voltage		−1900		−1950	mV	OE or DIR Low, V_{IN} = $V_{IH(Max)}$ or $V_{IL(Min)}$, Loading with 50Ω to −2V
V_{OHC}	Output HIGH Voltage Corner Point High	−1095		−1035		mV	V_{IN} = $V_{IH(Min)}$ or $V_{IL(Max)}$ Loading with 50Ω to −2V
V_{OLC}	Output LOW Voltage Corner Point Low		−1565		−1610	mV	
V_{IH}	Input HIGH Voltage	2.0	5.0	2.0	5.0	V	Over V_{TTL}, V_{EE}, T_C Range
V_{IL}	Input LOW Voltage	0	0.8	0	0.8	V	Over V_{TTL}, V_{EE}, T_C Range
I_{IH}	Input HIGH Current		70		70	µA	V_{IN} = +2.7V
	Breakdown Test		1.0		1.0	mA	V_{IN} = +5.5V
I_{IL}	Input LOW Current	−700		−700		µA	V_{IN} = +0.5V
V_{FCD}	Input Clamp Diode Voltage	−1.2		−1.2		V	I_{IN} = −18 mA
I_{EE}	V_{EE} Supply Current	−159 −169	−70 −70	−159 −169	−75 −75	mA	LE Low, OE and DIR High Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V

PCC ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −40°C to +85°C, C_L = 50 pF, V_{TTL} = +4.5V to +5.5V (Note)

Symbol	Parameter	T_C = −40°C		T_C = 0°C to +85°C		Units	Conditions
		Min	Max	Min	Max		
V_{OH}	Output HIGH Voltage	2.7 2.4		2.7 2.4		V V	I_{OH} = −3 mA, V_{TTL} = 4.75V I_{OH} = −3 mA, V_{TTL} = 4.50V
V_{OL}	Output LOW Voltage		0.5		0.5	V	I_{OL} = 24 mA, V_{TTL} = 4.50V
V_{IH}	Input HIGH Voltage	−1170	−870	−1165	−870	mV	Guaranteed HIGH Signal for All Inputs
V_{IL}	Input LOW Voltage	−1830	−1480	−1830	−1475	mV	Guaranteed LOW Signal for All Inputs
I_{IH}	Input HIGH Current		425		350	µA	V_{IN} = V_{IH} (Max)
I_{IH}	Input LOW Current	0.50		0.50		µA	V_{IN} = V_{IH} (Min)
I_{OZHT}	TRI-STATE Current Output High		70		70	µA	V_{OUT} = +2.7V
I_{OZLT}	TRI-STATE Current Output Low	−700		−700		µA	V_{OUT} = +0.5V
I_{OS}	Output Short-Circuit Current	−150	−60	−150	−60	mA	V_{OUT} = 0.0V, V_{TTL} = +5.5V
I_{TTL}	V_{TTL} Supply Current		74 49 67		74 49 67	mA mA mA	TTL Outputs LOW TTL Outputs HIGH TTL Outputs in TRI-STATE

Note: The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

Industrial Version (Continued)

PCC TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	T_C = −40°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	T_n to E_n (Transparent)	1.0	3.3	1.1	3.4	1.1	3.6	ns ns	*Figures 1 & 2*
t_{PLH} t_{PHL}	LE to E_n	1.7	3.4	1.7	3.5	1.9	3.7	ns ns	*Figures 1 & 2*
t_{PZH}	OE to E_n (Cutoff to High)	1.2	4.0	1.5	4.2	1.7	4.6	ns	*Figures 1 & 2*
t_{PHZ}	OE to E_n (High to Cutoff)	1.5	4.5	1.6	4.3	1.6	4.4	ns	*Figures 1 & 2*
t_{PHZ}	DIR to E_n (High to Cutoff)	1.6	4.1	1.6	4.1	1.7	4.3	ns	*Figures 1 & 2*
t_{set}	T_n to LE	2.5		1.0		1.0		ns	*Figures 1 & 2*
t_{hold}	T_n to LE	1.0		1.0		1.0		ns	*Figures 1 & 2*
t_{pw}(H)	Pulse Width LE	2.5		2.0		2.0		ns	*Figures 1 & 2*
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.4	2.3	0.6	1.6	0.6	1.6	ns	*Figures 1 & 2*

PCC ECL-to-TTL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, C_L = 50 pF

Symbol	Parameter	T_C = 0°C		T_C = 25°C		T_C = 85°C		Units	Conditions
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.3	5.4	2.4	5.4	2.6	5.7	ns	*Figures 3 & 4*
t_{PLH} t_{PHL}	LE to T_n	3.1	7.4	3.1	7.0	3.3	7.5	ns	*Figures 3 & 4*
t_{PZH} t_{PZL}	OE to T_n (Enable Time)	3.4 3.7	8.3 9.0	3.7 4.0	8.75 9.0	4.0 4.3	9.5 9.75	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	OE to T_n (Disable Time)	3.2 3.0	9.0 7.5	3.3 3.4	8.75 8.5	3.5 4.1	9.0 9.75	ns	*Figures 3 & 5*
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.7 2.8	8.0 7.3	2.6 3.1	8.5 7.75	3.1 4.0	8.75 9.0	ns	*Figures 3 & 6*
t_{set}	E_n to LE	2.5		1.0		1.0		ns	*Figures 3 & 4*
t_{hold}	E_n to LE	2.3		2.0		2.5		ns	*Figures 3 & 4*
t_{pw}(H)	Pulse Width LE	4.0		4.0		4.0		ns	*Figures 3 & 4*

Military Version

TTL-to-ECL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C, V_{TTL} = +4.5V to +5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions		Notes
V_{OH}	Output HIGH Voltage	−1025	−870	mV	0°C to +125°C	V_{IN} = V_{IH} (Max) or V_{IL} (Min)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085	−870	mV	−55°C			
V_{OL}	Output LOW Voltage	−1830	−1620	mV	0°C to +125°C			
		−1830	−1555	mV	−55°C			
	Cutoff Voltage		−1950	mV	0°C to +125°C	OE or DIR Low		
			−1850	mV	−55°C			
V_{OHC}	Output HIGH Voltage	−1035		mV	0°C to +125°C	V_{IN} = V_{IH} (Min) or V_{IL} (Max)	Loading with 50Ω to −2.0V	1, 2, 3
		−1085		mV	−55°C			
V_{OLC}	Output LOW Voltage		−1610	mV	0°C to +125°C			
			−1555	mV	−55°C			
V_{IH}	Input HIGH Voltage	2.0		V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		1, 2, 3, 4
V_{IL}	Input LOW Voltage		0.8	V	−55°C to +125°C	Over V_{TTL}, V_{EE}, T_C Range		1, 2, 3, 4
I_{IH}	Input HIGH Current		70	µA	−55°C to 125°C	V_{IN} = +2.7V		1, 2, 3
	Breakdown Test		1.0	mA	−55°C to +125°C	V_{IN} = +5.5V		
I_{IL}	Input LOW Current	−1.0		mA	−55°C to +125°C	V_{IN} = +0.5V		1, 2, 3
V_{FCD}	Input Clamp Diode Voltage	−1.2		V	−55°C to +125°C	I_{IN} = −18 mA		1, 2, 3
I_{EE}	V_{EE} Supply Current	−165 −175	−65 −65	mA	−55°C to +125°C	LE Low, OE and DIR High Inputs Open V_{EE} = −4.2V to −4.8V V_{EE} = −4.2V to −5.7V		1, 2, 3

Military Version (Continued)

ECL-to-TTL DC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{CC} = V_{CCA} = GND, T_C = −55°C to +125°C, C_L = 50 pF, V_{TTL} = +4.5V to + 5.5V

Symbol	Parameter	Min	Max	Units	T_C	Conditions	Notes
V_{OH}	Output HIGH Voltage	2.5 2.4		mV	0°C to +125°C −55°C	I_{OH} = −1 mA, V_{TTL} = 4.50V I_{OH} = −3 mA, V_{TTL} = 4.50V	1, 2, 3
V_{OL}	Output LOW Voltage		0.5	mV	−55°C +125°C	I_{OL} = 24 mA, V_{TTL} = 4.50V	
V_{IH}	Input HIGH Voltage	−1165	−870	mV	−55°C +125°C	Guaranteed HIGH Signal for All Inputs	1, 2, 3, 4
V_{IL}	Input LOW Voltage	−1830	−1475	mV	−55°C to +125°C	Guaranteed LOW Signal for All Inputs	1, 2, 3, 4
I_{IH}	Input HIGH Current		350 500	µA	0°C to +125°C	V_{EE} = −5.7V V_{IN} = V_{IH} (Max)	1, 2, 3
I_{IL}	Input LOW Current	0.50		µA	−55°C to +125°C	V_{EE} = −4.2V V_{IN} = V_{IL} (Min)	1, 2, 3
I_{OZHT}	TRI-STATE Current Output High		70	µA	−55°C to +125°C	V_{OUT} = +2.7V	1, 2, 3
I_{OZLT}	TRI-STATE Current Output Low	−1.0		mA	−55°C to +125°C	V_{OUT} = +0.5V	1, 2, 3
I_{OS}	Output Short-Circuit CURRENT	−150	−60	mA	−55°C to +125°C	V_{OUT} = 0.0V, V_{TTL} = +5.5V	1, 2, 3
I_{TTL}	V_{TTL} Supply Current		75 50 70	mA mA mA	−55°C to +125°C	TTL Outputs Low TTL Output High TTL Output in TRI-STATE	1, 2, 3

Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately without allowing for the junction temperature to stabilize due to heat dissipation after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at −55°C, +25°C, and +125°C, Subgroups, 1, 2 3, 7, and 8.

Note 3: Sample tested (Method 5005, Table I) on each manufactured lot at −55°C, +25°C, and +125°C, Subgroups A1, 2, 3, 7, and 8.

Note 4: Guaranteed by applying specified input condition and testing V_{OH}/V_{OL}.

TTL-to-ECL AC Electrical Characteristics

V_{EE} = −4.2V to −5.7V, V_{TTL} = +4.5V to +5.5V, V_{CC} = V_{CCA} = GND

Symbol	Parameter	T_C = −55°C		T_C = 25°C		T_C = +125°C		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	T_N to E_n (Transparent)	0.8	3.4	1.1	3.8	0.8	3.7	ns ns	*Figures 1 & 2*	1, 2, 3
t_{PLH} t_{PHL}	LE to E_n	1.2	3.8	1.4	3.7	1.1	3.8	ns ns	*Figures 1 & 2*	
t_{PZH}	OE to E_n (Cutoff to HIGH)	0.8	3.6	1.5	4.0	2.0	5.2	ns	*Figures 1 & 2*	1, 2, 3
t_{PHZ}	OE to E_n (HIGH to Cutoff)	1.5	4.6	1.6	4.2	1.6	4.3	ns	*Figures 1 & 2*	
t_{PHZ}	DIR to E_n (HIGH to Cutoff)	1.6	4.7	1.6	4.3	1.7	4.3	ns	*Figures 1 & 2*	
t_{set}	T_n to LE	2.5		2.0		2.5		ns	*Figures 1 & 2*	4
t_{hold}	T_n to LE	2.5		2.0		2.5		ns	*Figures 1 & 2*	
t_{pw}(H)	Pulse Width LE	2.5		2.0		2.5		ns	*Figures 1 & 2*	4
t_{TLH} t_{THL}	Transition Time 20% to 80%, 80% to 20%	0.4	2.3	0.5	2.1	0.4	2.4	ns	*Figures 1 & 2*	4

Military Version (Continued)

ECL-to-TTL AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{TTL} = +4.5V$ to $+5.5V$, $V_{CC} = V_{CCA} = GND$, $C_L = 50$ pF

Symbol	Parameter	$T_C = -55°C$		$T_C = 25°C$		$T_C = +125°C$		Units	Conditions	Notes
		Min	Max	Min	Max	Min	Max			
t_{PLH} t_{PHL}	E_n to T_n (Transparent)	2.1	6.0	2.0	5.6	2.2	6.3	ns	*Figures 3 & 4*	1, 2, 3
t_{PLH} t_{PHL}	LE to T_n	3.1	7.0	3.1	6.5	3.3	7.5	ns	*Figures 3 & 4*	
t_{PZH} t_{PZL}	$\overline{OE}$ to T_n (Enable Time)	3.2 3.6	8.0 8.0	3.7 4.0	8.0 8.5	4.0 4.3	9.2 9.6	ns	*Figures 3 & 5*	1, 2, 3
t_{PHZ} t_{PLZ}	$\overline{OE}$ to T_n (Disable Time)	3.2 3.0	8.5 8.0	3.3 3.4	8.0 7.5	3.5 4.1	8.4 10.0	ns	*Figures 3 & 5*	
t_{PHZ} t_{PLZ}	DIR to T_n (Disable Time)	2.6 2.7	7.0 7.0	2.6 3.1	7.0 7.0	2.9 4.0	8.0 10.0	ns	*Figures 3 & 6*	
t_{set}	E_n to LE	2.5		2.0		2.5		ns	*Figures 3 & 4*	4
t_{hold}	E_n to LE	3.0		2.5		3.0		ns	*Figures 3 & 4*	
$t_{pw}(H)$	Pulse Width LE	2.5		2.0		5.0		ns	*Figures 3 & 4*	4

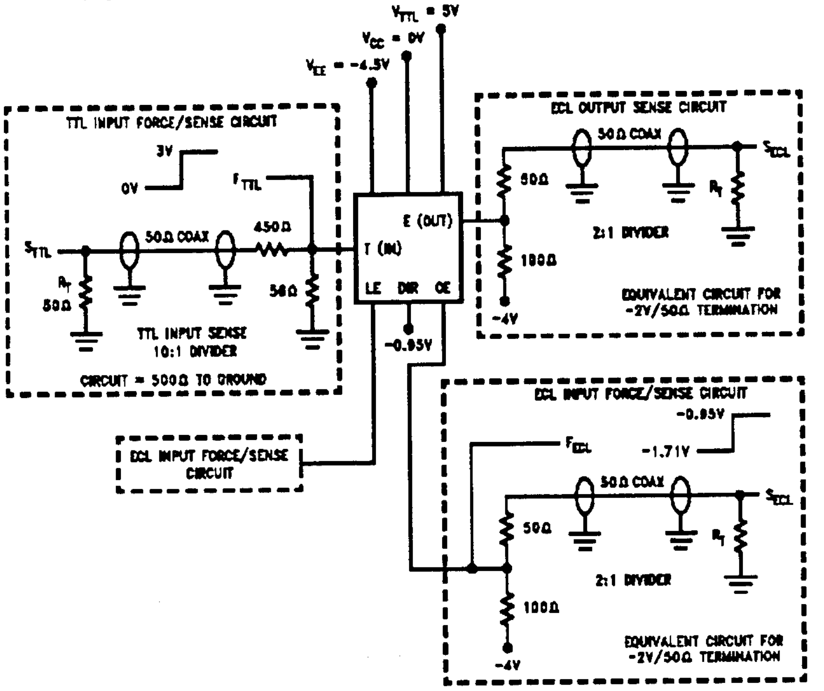
Note 1: F100K 300 Series cold temperature testing is performed by temperature soaking (to guarantee junction temperature equals −55°C), then testing immediately after power-up. This provides "cold start" specs which can be considered a worst case condition at cold temperatures.

Note 2: Screen tested 100% on each device at +25°C, temperature only, Subgroup A9.

Note 3: Sample tested (Method 5005, Table I) on each mfg. lot at +25°C, Subgroup A9, and at +125°C and −55°C temperatures, Subgroups A10 and A11.

Note 4: Not tested at +25°C, +125°C and −55°C temperature (design characterization data).

Test Circuitry (TTL-to-ECL)



TL/F/10219–7

Note 1: R_T = 50Ω termination. When an input or output is being monitored by a scope, R_T is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_T.

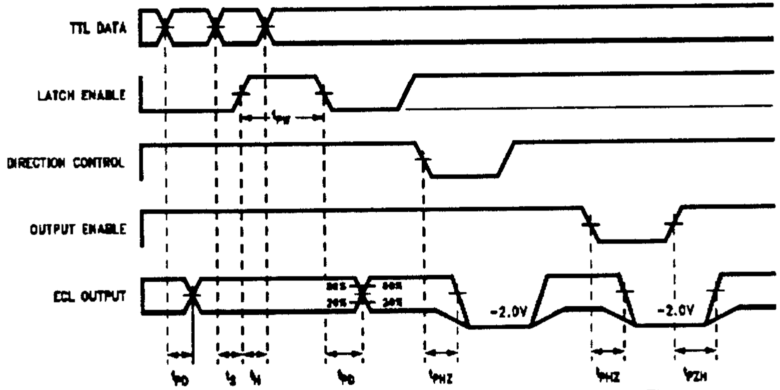
Note 2: TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

Note 3: V_{TTL} is decoupled to ground with 0.1 μF to ground, V_{EE} is decoupled to ground with 0.01 μF and V_{CC} is connected to ground.

Note 4: For ECL input pins, the equivalent force/sense circuitry is optional.

FIGURE 1. TTL-to-ECL AC Test Circuit

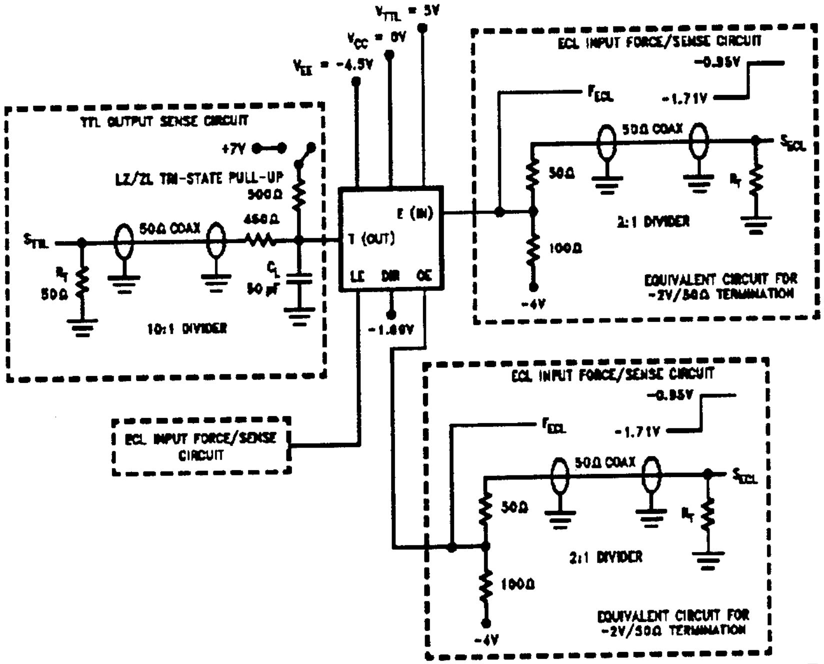
Switching Waveforms (TTL-to-ECL)



TL/F/10219–9

FIGURE 2. TTL to ECL Transition—Propagation Delay and Transition Times

Test Circuitry (ECL-to-TTL)



TL/F/10219-10

Note 1: R_t = 50Ω termination. When an input or output is being monitored by a scope, R_t is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, an external 50Ω resistance must be applied to serve as R_t.

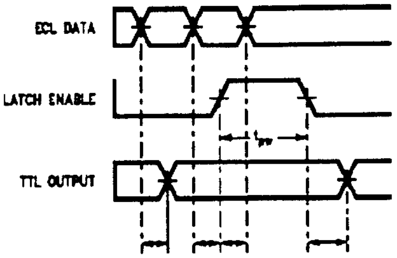
Note 2: The TTL Tri-State pull up switch is connected to +7V only for ZL and LZ tests.

Note 3: TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

Note 4: V_{TTL} is decoupled to ground with 0.1 μF, V_{EE} is decoupled to ground with 0.01 μF and V_{CC} is connected to ground.

FIGURE 3. ECL-to-TTL AC Test Circuit

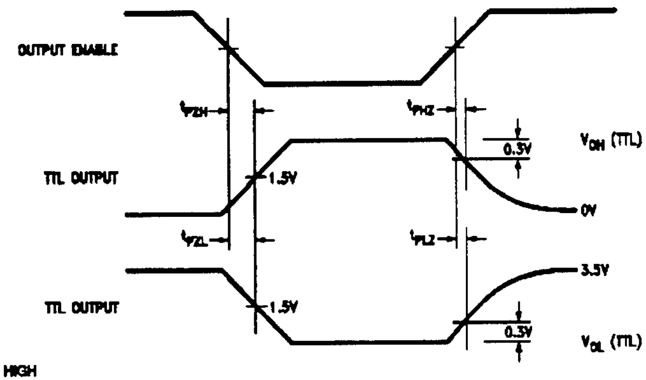
Switching Waveforms (ECL-to-TTL)



TL/F/10219-11

Note: DIR is LOW, and OE is HIGH

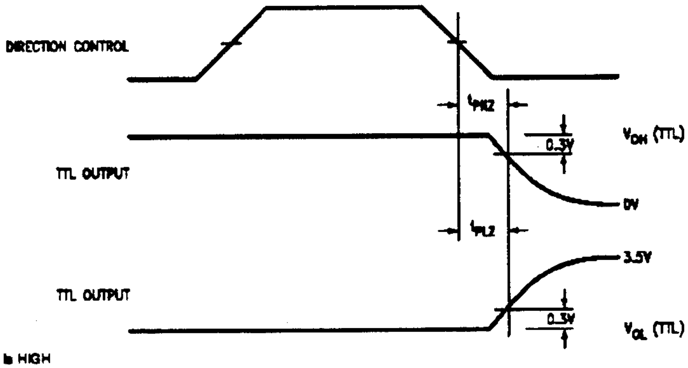
FIGURE 4. ECL-to-TTL Transition—Propagation Delay and Transition Times



Note: DIR is LOW, LE is HIGH

TL/F/10219-14

FIGURE 5. ECL-to-TTL Transition, OE to TTL Output, Enable and Disable Times

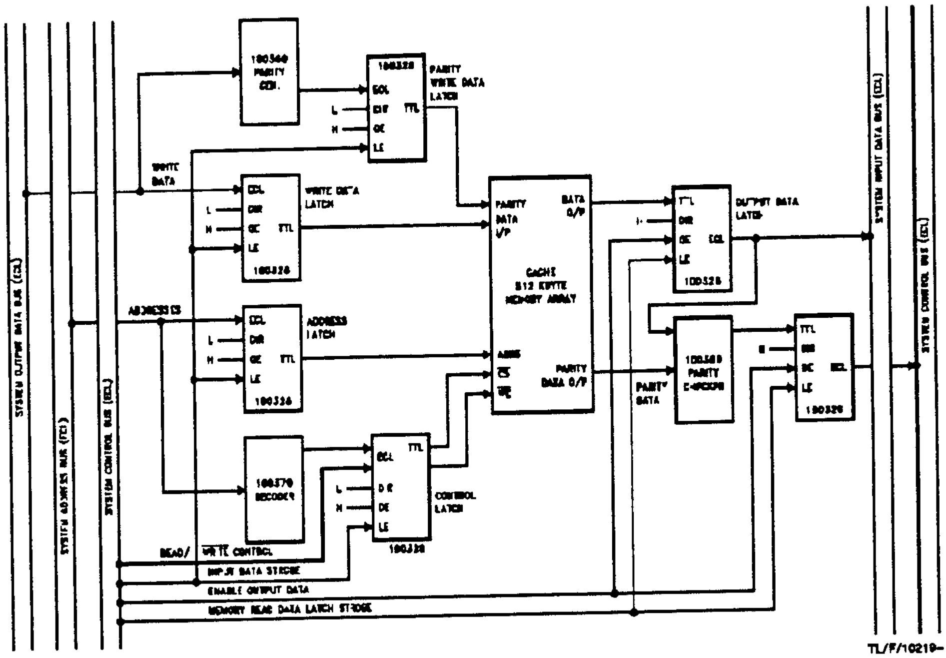


Note: OE is HIGH, LE is HIGH

TL/F/10219-16

FIGURE 6. ECL-to-TTL Transition, DIR to TTL Output, Disable Time

Applications



TL/F/10219-12

FIGURE 7. Applications Diagram—MOS/TTL SRAM Interface Using 100328 ECL-TTL Latched Translator

Ordering Information

The device number is used to form part of a simplified purchasing code where A package type and temperature range are defined as follows:

100328 D C QB

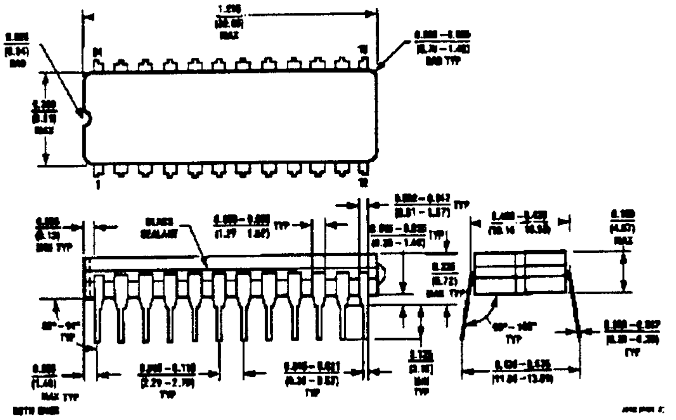
Device Type (Basic) — 100328

Package Code — D
D = Ceramic DIP
F = Quad Cerpak
P = Plastic DIP
Q = Plastic Leaded Chip Carrier (PCC)
S = Small Outline (SOIC)

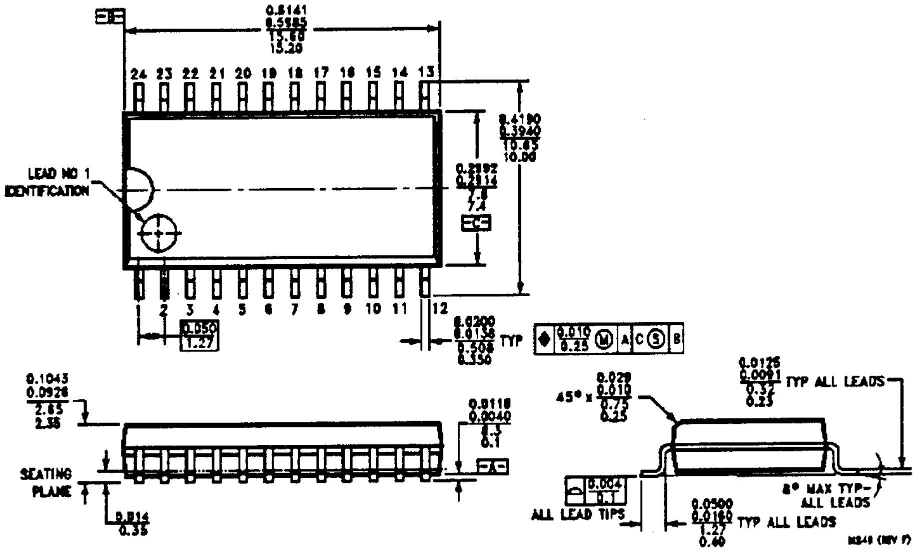
Temperature Range — C
C = Commercial (0°C to +85°C)
I = Industrial (−40°C to +85°C) (PCC Only)
M = Military (−55°C to +125°C)

Special Variation — QB
QB = Military grade device with environmental and burn-in processing

Physical Dimensions inches (millimeters)

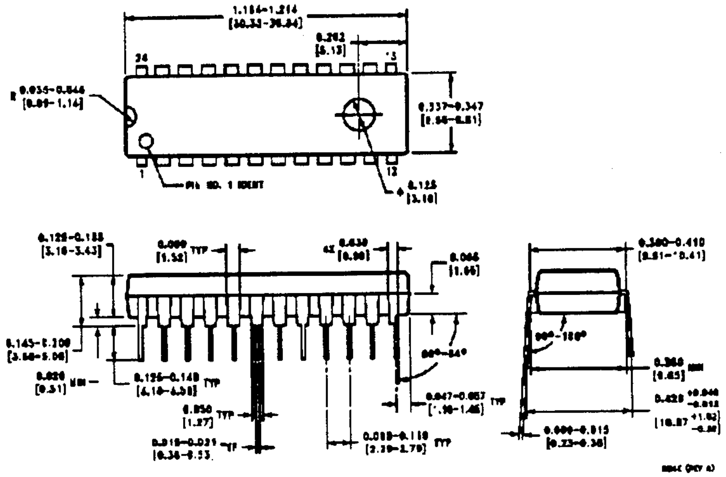


24-Lead Ceramic Dual-In-Line Package (0.400" Wide) (D)
NS Package Number J24E

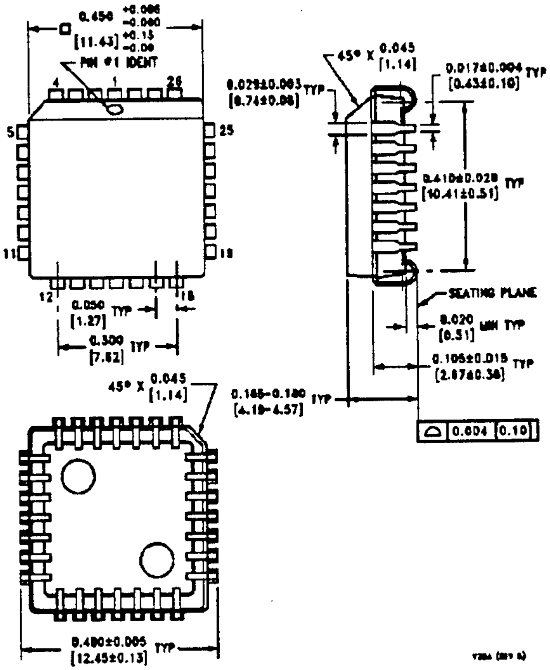


24-Lead Molded Package (0.300" Wide) (S)
NS Package Number M24B

Physical Dimensions inches (millimeters) (Continued)

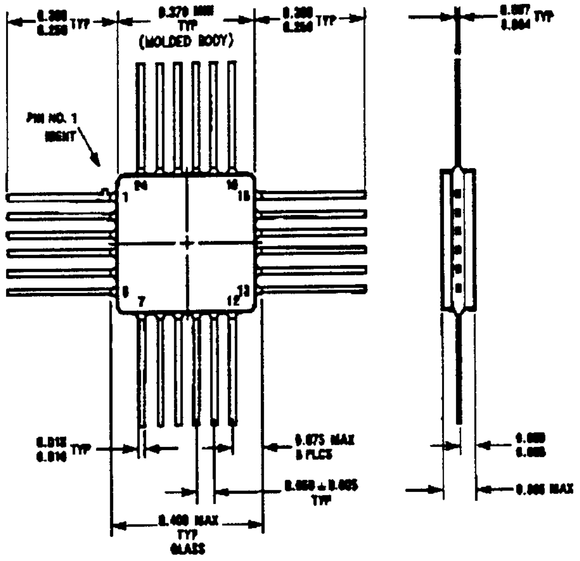


24-Lead Plastic Dual-In-Line Packakge (P)
NS Package Number N24E



28-Lead Plastic Chip Carrier (V)
NS Package Number V28A

Physical Dimensions inches (millimeters) (Continued)



24-Lead Quad Cerpak (F)
NS Package Number W24B

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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HARRIS
SEMICONDUCTOR

HCS138MS

Radiation Hardened Inverting 3-to-8 Line Decoder/Demultiplexer

August 1995

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K RAD (Si)
- SEP Effective LET No Upsets: >100 MEV-cm^2/mg
- Single Event Upset (SEU) Immunity < 2 x 10^{-9} Errors/ Bit-Day (Typ)
- Dose Rate Survivability: >1 x 10^{12} RAD (Si)/s
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Standard Outputs - 10 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5µA at VOL, VOH

Description

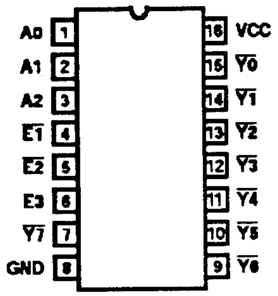
The Harris HCS138MS is a Radiation Hardened 3-to-8 line Decoder/Demultiplexer. The outputs are active in the low state. Two active low and one active high enables ($\overline{E1}$, $\overline{E2}$, E3) are provided. If the device is enabled, the binary inputs (A0, A1, A2) determine which one of the eight normally high outputs will go to a low logic level.

The HCS138MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

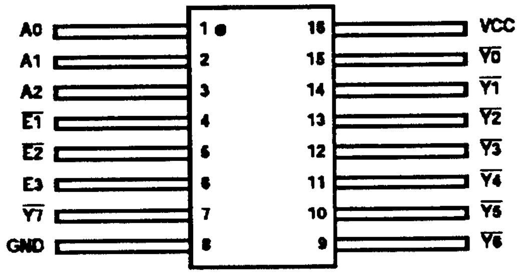
The HCS138MS is supplied in a 16 lead Ceramic flatpack (K suffix) or a SBDIP Package (D suffix).

Pinouts

16 LEAD CERAMIC DUAL-IN-LINE
METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T16
TOP VIEW



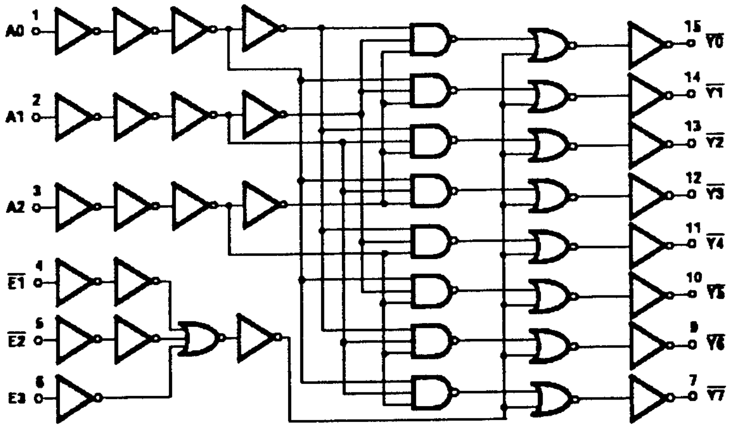
16 LEAD CERAMIC METAL SEAL
FLATPACK PACKAGE (FLATPACK)
MIL-STD-1835 CDFP4-F16
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HCS138DMSR	-55°C to +125°C	Harris Class S Equivalent	16 Lead SBDIP
HCS138KMSR	-55°C to +125°C	Harris Class S Equivalent	16 Lead Ceramic Flatpack
HCS138D/Sample	+25°C	Sample	16 Lead SBDIP
HCS138K/Sample	+25°C	Sample	16 Lead Ceramic Flatpack
HCS138HMSR	+25°C	Die	Die

Functional Diagram



TRUTH TABLE

INPUTS						OUTPUTS							
ENABLE													
E3	$\overline{E2}$	$\overline{E1}$	A2	A1	A0	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$
X	X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	H	L	H	H	H	H
H	L	L	H	L	L	H	H	H	H	L	H	H	H
H	L	L	H	L	H	H	H	H	H	H	L	H	H
H	L	L	H	H	L	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings

Supply Voltage (VCC) .... -0.5V to +7.0V
Input Voltage Range, All Inputs .... -0.5V to VCC +0.5V
DC Input Current, Any One Input .... ±10mA
DC Drain Current, Any One Output .... ±25mA
(All Voltage Reference to the VSS Terminal)
Storage Temperature Range (TSTG) .... -65°C to +150°C
Lead Temperature (Soldering 10sec) .... +265°C
Junction Temperature (TJ) .... +175°C
ESD Classification .... Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	73°C/W	24°C/W
Ceramic Flatpack Package	114°C/W	29°C/W

Maximum Package Power Dissipation at +125°C Ambient
SBDIP Package 0.68W
Ceramic Flatpack Package 0.44W

If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:
SBDIP Package .... 13.7mW/°C
Ceramic Flatpack Package .... 8.8mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage .... +4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF) .... 500ns Max
Operating Temperature Range (T_A) .... -55°C to +125°C
Input Low Voltage (VIL) .... 0.0V to 30% of VCC
Input High Voltage (VIH) .... 70% of VCC to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50µA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50µA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Address to Output	TPLH	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	34	ns
	TPHL	VCC = 4.5V	9	+25°C	2	28	ns
			10, 11	+125°C, -55°C	2	34	ns
Enable to Output	TPLH	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	33	ns
	TPHL	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	33	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	-	78	pF
			1	+125°C	-	113	pF
Input Capacitance	CIN	VCC = 5.0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	15	ns
			1	+125°C	-	22	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS MIN	200K RAD LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	mA

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS		UNITS
				MIN	MAX	
Output Voltage Low	VOL	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC), IOL = 50µA	+25°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V and 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC), IOH = -50µA	+25°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC), (Note 3)	+25°C	-	-	-
Address to Output	TPLH	VCC = 4.5V	+25°C	2	34	ns
	TPHL	VCC = 4.5V	+25°C	2	34	ns
Enable to Output	TPLH	VCC = 4.5V	+25°C	2	33	ns
	TPHL	VCC = 4.5V	+25°C	2	33	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 7, 9	

NOTE:

1. Alternate group A inspection in accordance with method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:
1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
7, 9 - 15	1 - 6, 8		16		
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
7, 9 - 15	8	-	1 - 6, 16	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	4, 5, 8	7, 9 - 15	3, 6, 16	2	1

NOTES:
1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
7, 9 - 15	8	1 - 6, 16

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing.
Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Harris Space Level Product Flow - 'MS'

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 24 hrs. min., +125°C min., Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% Static Burn-In 2, Condition A or B, 24 hrs. min., +125°C min., Method 1015

100% Interim Electrical Test 2 (T2)

100% Delta Calculation (T0-T2)

100% PDA 1, Method 5004 (Notes 1and 2)

100% Dynamic Burn-In, Condition D, 240 hrs., +125°C or Equivalent, Method 1015

100% Interim Electrical Test 3 (T3)

100% Delta Calculation (T0-T3)

100% PDA 2, Method 5004 (Note 2)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic, Method 2012 (Note 3)

100% External Visual, Method 2009

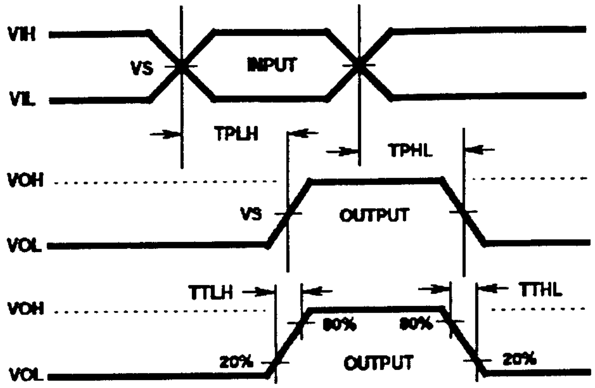
Sample - Group A, Method 5005 (Note 4)

100% Data Package Generation (Note 5)

NOTES:

1. Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
2. Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Data Package Contents:
   - Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
   - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
   - X-Ray report and film. Includes penetrometer measurements.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Lot Serial Number Sheet (Good units serial number and lot number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

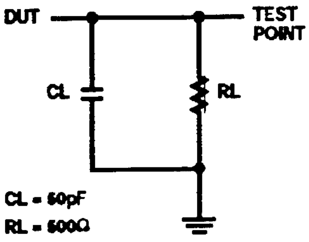
AC Timing Diagrams



AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



Die Characteristics

DIE DIMENSIONS:
85 x 101 mils

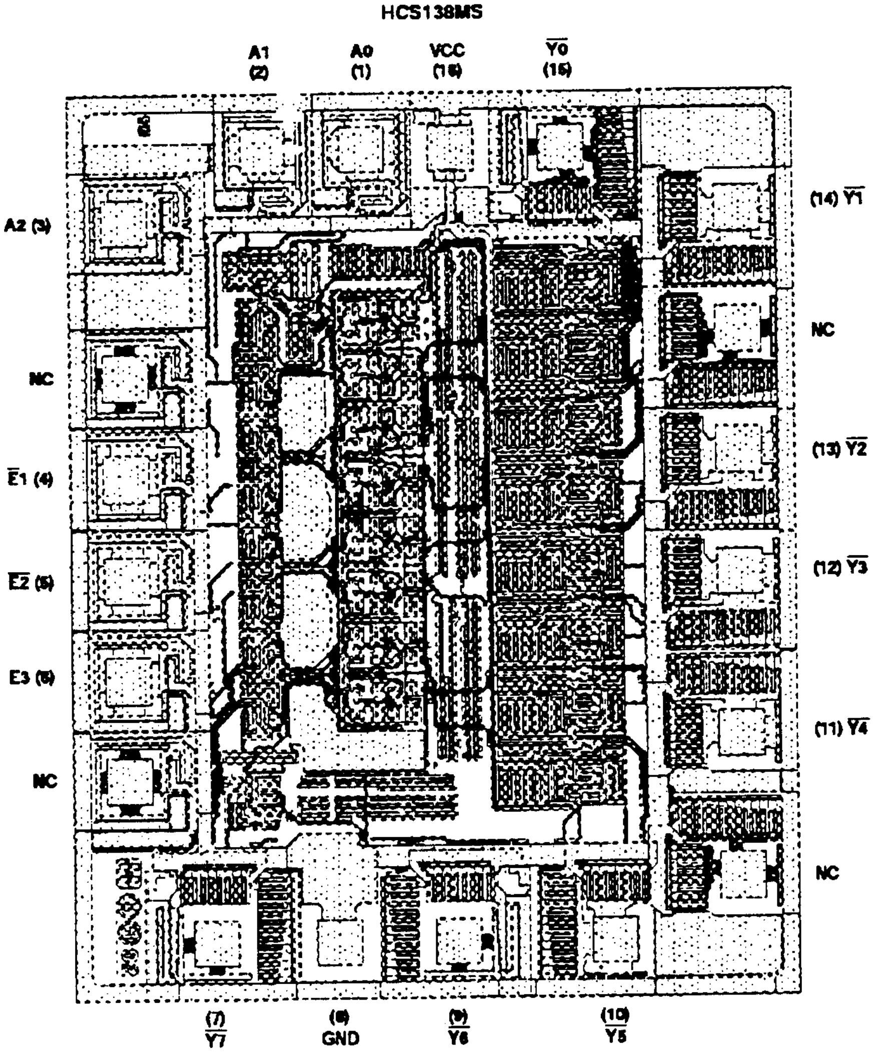
METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100μm x 100μm
4 x 4 mils

Metallization Mask Layout



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCS138 is TA14361A.

HARRIS
SEMICONDUCTOR

HCS573MS

Radiation Hardened Octal Transparent Latch, Three-State

September 1995

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K RAD (Si)
- SEP Effective LET No Upsets: >100 MEV-cm^2/mg
- Single Event Upset (SEU) Immunity < 2 x 10^{-9} Errors/Bit-Day (Typ)
- Dose Rate Survivability: >1 x 10^{12} RAD (Si)/s
- Dose Rate Upset >10^{10} RAD (Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 0.3 VCC Max
  - VIH = 0.7 VCC Min
- Input Current Levels Ii ≤ 5µA at VOL, VOH

Description

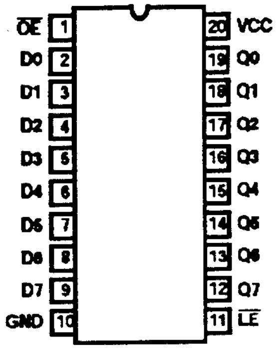
The Harris HCS573MS is a Radiation Hardened octal transparent three-state latch with an active low output enable. The HCS573MS utilizes advanced CMOS/SOS technology. The outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the tri-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high impedance state. The latch operation is independent of the state of the Output Enable.

The HCS573MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

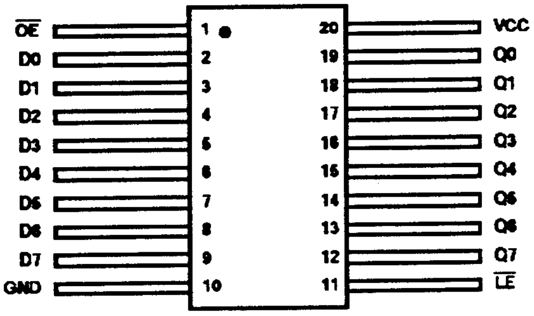
The HCS573MS is supplied in a 20 lead Ceramic flatpack (K suffix) or a SBDIP Package (D suffix).

Pinouts

20 LEAD CERAMIC DUAL-IN-LINE
METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T20, LEAD FINISH C
TOP VIEW



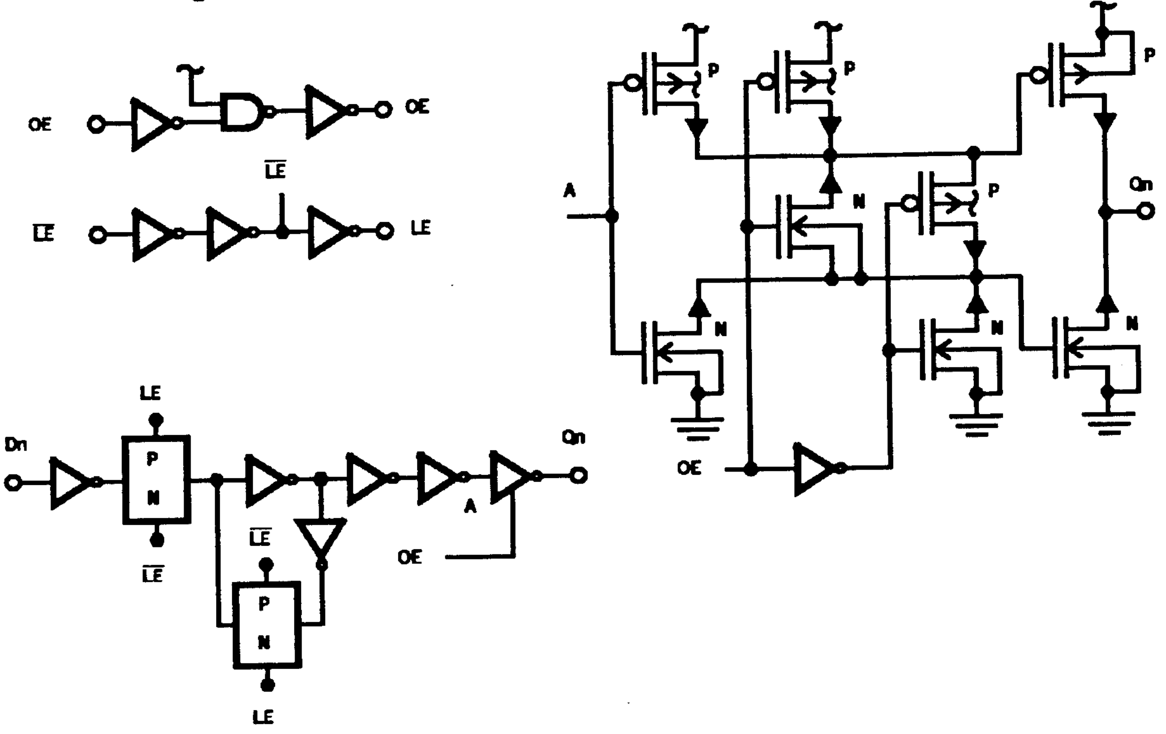
20 LEAD CERAMIC METAL SEAL
FLATPACK PACKAGE (FLATPACK)
MIL-STD-1835 CDFP4-F20, LEAD FINISH C
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HCS573DMSR	-55°C to +125°C	Harris Class S Equivalent	20 Lead SBDIP
HCS573KMSR	-55°C to +125°C	Harris Class S Equivalent	20 Lead Ceramic Flatpack
HCS573D/Sample	+25°C	Sample	20 Lead SBDIP
HCS573K/Sample	+25°C	Sample	20 Lead Ceramic Flatpack
HCS573HMSR	+25°C	Die	Die

Functional Diagram



TRUTH TABLE

$\overline{\text{OUTPUT ENABLE}}$	$\overline{\text{LATCH ENABLE}}$	DATA	OUTPUT
L	H	H	H
L	H	L	L
L	L	l	L
L	L	h	H
H	X	X	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance
l = Low voltage level prior to the high-to-low latch enable transition
h = High voltage level prior to the high-to-low latch enable transition

Absolute Maximum Ratings

Supply Voltage (VCC)	-0.5V to +7.0V
Input Voltage Range, All Inputs	-0.5V to VCC +0.5V
DC Input Current, Any One Input	±10mA
DC Drain Current, Any One Output	±25mA
(All Voltage Reference to the VSS Terminal)	
Storage Temperature Range (TSTG)	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+265°C
Junction Temperature (TJ)	+175°C
ESD Classification	Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	72°C/W	24°C/W
Ceramic Flatpack Package	107°C/W	28°C/W

Maximum Package Power Dissipation at +125°C Ambient

SBDIP Package	0.69W
Ceramic Flatpack Package	0.47W

If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:

SBDIP Package	13.9mW/°C
Ceramic Flatpack Package	9.3mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permenent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation..

Operating Conditions

Supply Voltage (VCC)	+4.5V to +5.5V
Input Rise and Fall Times at VCC = 4.5V (TR, TF)	500ns Max
Operating Temperature Range (T_A)	-55°C to +125°C
Input Low Voltage (VIL)	0.0V to 30% of VCC
Input High Voltage (VIH)	70% of VCC to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	μA
			2, 3	+125°C, -55°C	-	750	μA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 3.15V, IOL = 50μA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 3.85V, IOL = 50μA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 3.15V, IOH = -50μA, VIL = 1.35V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 3.85V, IOH = -50μA, VIL = 1.65V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	μA
			2, 3	+125°C, -55°C	-	±5.0	μA
Output Leakage Current	IOZ	VCC = 5.5V, VIN = 0V or VCC	1	+25°C	-	±1.0	μA
			2, 3	+125°C, -55°C	-	±50	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC) (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages reference to device GND.
2. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Data to Qn	TPLH TPHL	VCC = 4.5V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	29	ns
$\overline{LE}$ to Qn	TPLH	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	35	ns
	TPHL	VCC = 4.5V	9	+25°C	2	31	ns
			10, 11	+125°C, -55°C	2	40	ns
Enable to Output	TPZL	VCC = 4.5V	9	+25°C	2	27	ns
			10, 11	+125°C, -55°C	2	33	ns
	TPZH	VCC = 4.5V	9	+25°C	2	24	ns
			10, 11	+125°C, -55°C	2	29	ns
Disable to Output	TPLZ	VCC = 4.5V	9	+25°C	2	25	ns
			10, 11	+125°C, -55°C	2	29	ns
	TPHZ	VCC = 4.5V	9	+25°C	2	21	ns
			10, 11	+125°C, -55°C	2	25	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	-	30	pF
			1	+125°C, -55°C	-	60	pF
Input Capacitance	CIN	VCC = 5.0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C, -55°C	-	10	pF
Output Transition Time	TTHL TTLH	VCC = 4.5V	1	+25°C	-	12	ns
			1	+125°C, -55°C	-	18	ns
Setup Time Data to $\overline{LE}$	TSU	VCC = 4.5V	1	+25°C	10	-	ns
			1	+125°C, -55°C	15	-	ns
Hold Time Data to $\overline{LE}$	TH	VCC = 4.5V	1	+25°C	8	-	ns
			1	+125°C, -55°C	12	-	ns
Pulse Width $\overline{LE}$	TW	VCC = 4.5V	1	+25°C	16	-	ns
			1	+125°C, -55°C	24	-	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS		UNITS
				MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC), IOL = 50µA	+25°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = 0.70(VCC), VIL = 0.30(VCC), IOH = -50µA	+25°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	µA
Tri-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC, VCC = 5.5V	+25°C	-	±50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 0.70(VCC), VIL = 0.30(VCC), (Note 3)	+25°C	-	-	-
Data to Qn	TPHL TPLH	VCC = 4.5V	+25°C	2	29	ns
LEN to Qn	TPLH	VCC = 4.5V	+25°C	2	35	ns
	TPHL	VCC = 4.5V	+25°C	2	40	ns
Enable to Output	TPZL	VCC = 4.5V	+25°C	2	33	ns
	TPZH	VCC = 4.5V	+25°C	2	29	ns
Disable to Output	TPLZ	VCC = 4.5V	+25°C	2	29	ns
	TPHZ	VCC = 4.5V	+25°C	2	25	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = VCC.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12µA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11, (Note 2)
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 7, 9	

NOTES:

1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.
2. Table 5 parameters only.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 6V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
12 - 19	1 - 11	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
12 - 19	10	-	1 - 9, 11, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	1, 10	12 - 19	20	11	2 - 9

NOTES:

1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
12 - 19	10	1 - 9, 11, 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing.
Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Harris Space Level Product Flow - 'MS'

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 24 hrs. min., +125°C min., Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% Static Burn-In 2, Condition A or B, 24 hrs. min., +125°C min., Method 1015

100% Interim Electrical Test 2 (T2)

100% Delta Calculation (T0-T2)

100% PDA 1, Method 5004 (Notes 1and 2)

100% Dynamic Burn-In, Condition D, 240 hrs., +125°C or Equivalent, Method 1015

100% Interim Electrical Test 3 (T3)

100% Delta Calculation (T0-T3)

100% PDA 2, Method 5004 (Note 2)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic, Method 2012 (Note 3)

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 4)

100% Data Package Generation (Note 5)

NOTES:

1. Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
2. Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Data Package Contents:
   - Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
   - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
   - X-Ray report and film. Includes penetrometer measurements.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Lot Serial Number Sheet (Good units serial number and lot number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

AC Timing Diagrams

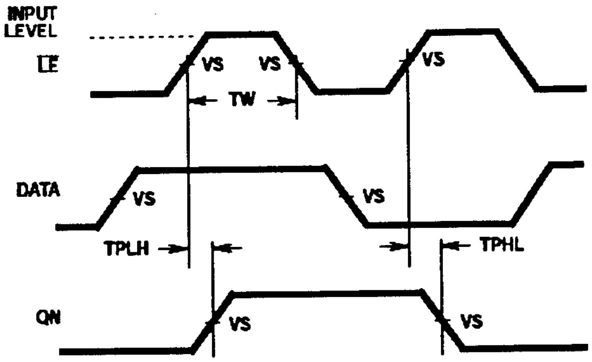


FIGURE 1. LATCH ENABLE PROPAGATION DELAYS

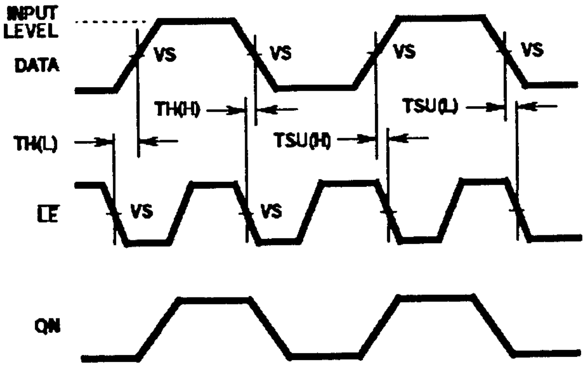


FIGURE 2. LATCH ENABLE PREREQUISITE TIMES

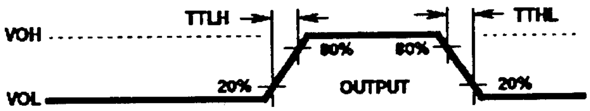
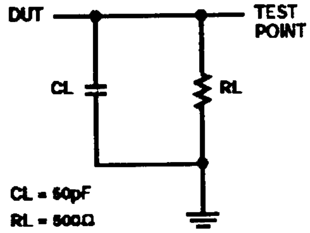


FIGURE 3. DATA SET-UP AND HOLD TIMES

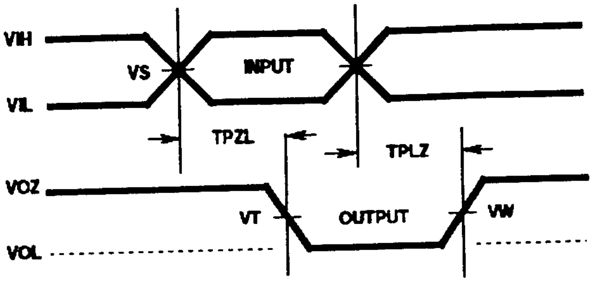
AC VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

AC Load Circuit



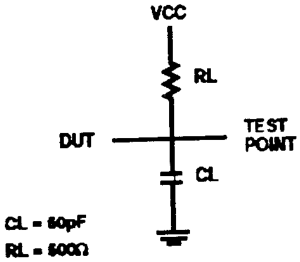
Three-State Low Timing Diagram



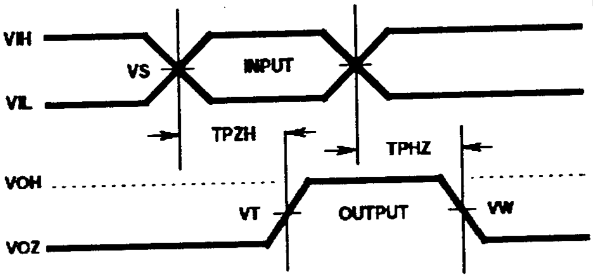
THREE-STATE LOW VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.90	V
GND	0	V

Three-State Low Load Circuit



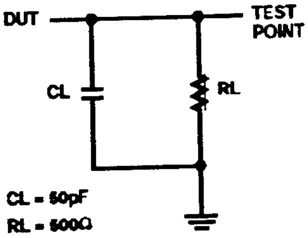
Three-State HighTiming Diagram



THREE-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	3.60	V
GND	0	V

Three-State High Load Circuit



Die Characteristics

DIE DIMENSIONS:
101 x 85 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

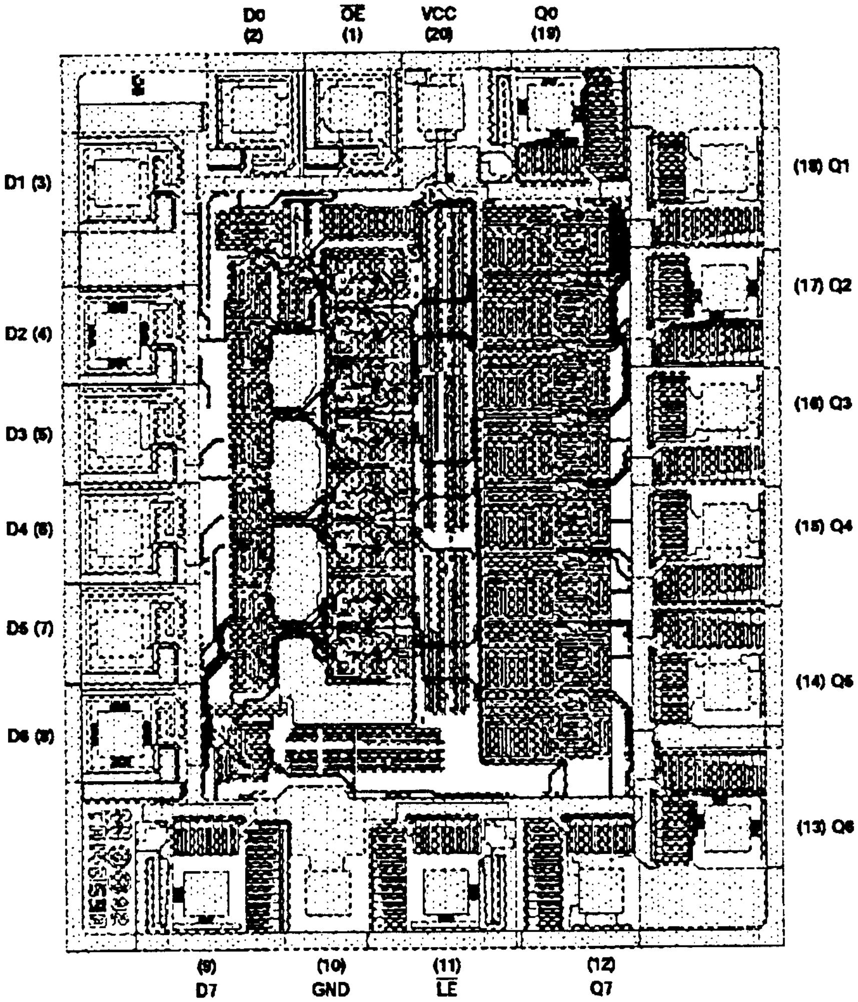
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100µm x 100µm
4 x 4 mils

Metallization Mask Layout

HCS573MS



HARRIS
SEMICONDUCTOR

HCTS541MS

Radiation Hardened Non-Inverting Octal Buffer/Line Driver, Three-State

August 1995

Features

- 3 Micron Radiation Hardened CMOS SOS
- Total Dose 200K RAD (Si)
- SEP Effective LET No Upsets: >100 MEV-cm^2/mg
- Single Event Upset (SEU) Immunity < 2 x 10^{-9} Errors/Bit-Day (Typ)
- Dose Rate Survivability: >1 x 10^{12} RAD (Si)/s
- Dose Rate Upset >10^{10} RAD (Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Fanout (Over Temperature Range)
  - Bus Driver Outputs - 15 LSTTL Loads
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
  - VIL = 0.8V Max
  - VIH = VCC/2 Min
- Input Current Levels Ii ≤ 5μA at VOL, VOH

Description

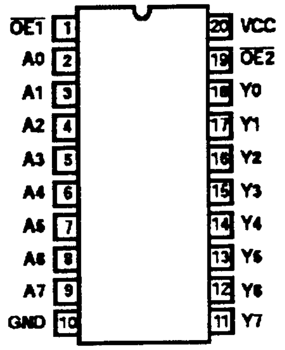
The Harris HCTS541MS is a Radiation Hardened non-inverting octal buffer/line driver, three-state outputs. The output enable pins (OEN1 and OEN2) control the three-state outputs. If either enable is high the outputs will be in the high impedance state. For data output both enables (OEN1 and OEN2) must be low.

The HCTS541MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

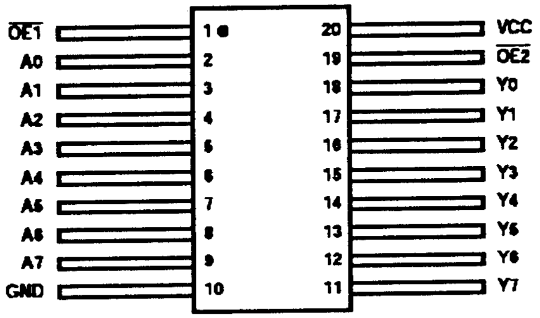
The HCTS54 is supplied in a 20 lead Ceramic flatpack (K suffix) or a SBDIP Package (D suffix).

Pinouts

20 LEAD CERAMIC DUAL-IN-LINE
METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T20
TOP VIEW



20 LEAD CERAMIC METAL SEAL
FLATPACK PACKAGE (FLATPACK)
MIL-STD-1835 CDFP4-F20
TOP VIEW

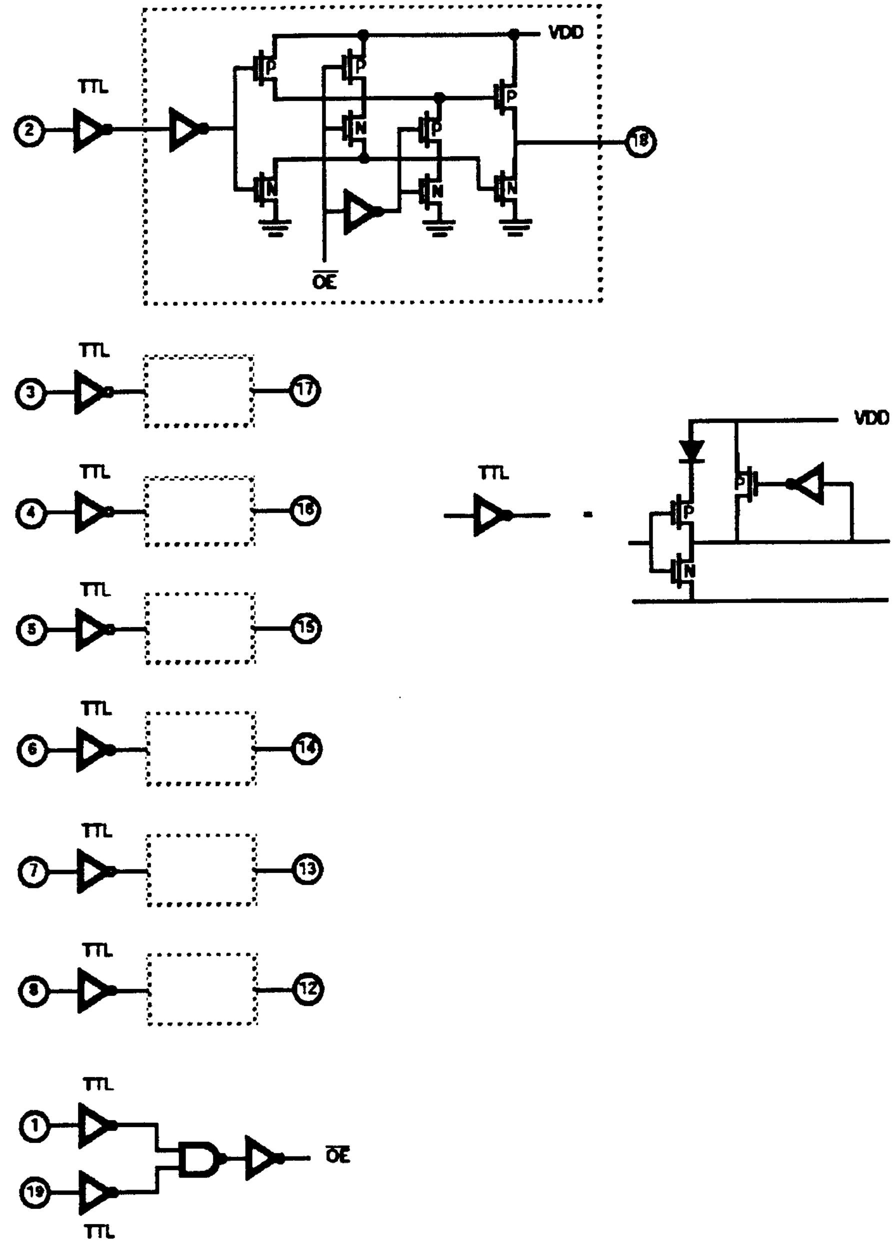


Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HCTS541DMSR	-55°C to +125°C	Harris Class S Equivalent	20 Lead SBDIP
HCTS541KMSR	-55°C to +125°C	Harris Class S Equivalent	20 Lead Ceramic Flatpack
HCTS541D/Sample	+25°C	Sample	20 Lead SBDIP
HCTS541K/Sample	+25°C	Sample	20 Lead Ceramic Flatpack
HCTS541HMSR	+25°C	Die	Die

Spec Number **518630**
File Number **3073.1**

Functional Block Diagram



TRUTH TABLE

INPUTS			OUTPUTS
$\overline{OE1}$	$\overline{OE2}$	An	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = High Voltage Level, L = Low Voltage Level, X = Immaterial, Z = High Impedance

Absolute Maximum Ratings

Supply Voltage (VCC)	-0.5 to +7.0V
Input Voltage Range, All Inputs	-0.5V to VCC +0.5V
DC Input Current, Any One Input	±10mA
DC Drain Current, Any One Output	±25mA
(All Voltage Reference to the VSS Terminal)	
Storage Temperature Range (TSTG)	-65°C to +150°C
Lead Temperature (Soldering 10sec)	+265°C
Junction Temperature (TJ)	+175°C
ESD Classification	Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	72°C/W	24°C/W
Ceramic Flatpack Package	107°C/W	28°C/W

Maximum Package Power Dissipation at +125°C Ambient

SBDIP Package	0.69W
Ceramic Flatpack Package	0.47W

If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:

SBDIP Package	13.9mW/°C
Ceramic Flatpack Package	9.3mW/°C

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage (VCC)	+4.5V to +5.5V
Operating Temperature Range (T_A)	-55°C to +125°C
Input Rise and Fall Times at 4.5V VCC (TR, TF)	500ns Max
Input Low Voltage (VIL)	0.0V to 0.8V
Input High Voltage (VIH)	VCC/2 to VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	40	µA
			2, 3	+125°C, -55°C	-	750	µA
Output Current (Sink)	IOL	VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V	1	+25°C	7.2	-	mA
			2, 3	+125°C, -55°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V	1	+25°C	-7.2	-	mA
			2, 3	+125°C, -55°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V, VIH = 2.25V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 5.5V, VIH = 2.75V, IOL = 50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V, VIH = 2.25V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 5.5V, VIH = 2.75V, IOH = -50µA, VIL = 0.8V	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±5.0	µA
Three-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC, VCC = 5.5V	1	+25°C	-	±1	µA
			2, 3	+125°C, -55°C	-	±50	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	-

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Data to Output	TPHL, TPLH	VCC = 4.5V	9	+25°C	2	20	ns
		VCC = 4.5V	10, 11	+125°C, -55°C	2	22	ns
Enable to Output	TPZL	VCC = 4.5V	9	+25°C	2	23	ns
			10, 11	+125°C, -55°C	2	26	ns
	TPZH	VCC = 4.5V	9	+25°C	2	20	ns
			10, 11	+125°C, -55°C	2	21	ns
Disable to Output	TPLZ	VCC = 4.5V	9	+25°C	2	22	ns
			10, 11	+125°C, -55°C	2	23	ns
	TPHZ	VCC = 4.5V	9	+25°C	2	21	ns
			10, 11	+125°C, -55°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Capacitance Power Dissipation	CPD	VCC = 5.0V, f = 1MHz	1	+25°C	-	38	pF
			1	+125°C, -55°C	-	60	pF
Input Capacitance	CIN	VCC = 5.0V, f = 1MHz	1	+25°C	-	10	pF
			1	+125°C	-	10	pF
Output Transition Time	TTHL, TTLH	VCC = 4.5V	1	+25°C	-	12	ns
			1	+125°C, -55°C	-	18	ns

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	TEMPERATURE	200K RAD LIMITS		UNITS
				MIN	MAX	
Quiescent Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	0.75	mA
Output Current (Sink)	IOL	VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V	+25°C	6.0	-	mA
Output Current (Source)	IOH	VCC = 4.5V, VIN = VCC or GND, VOUT = VCC -0.4V	+25°C	-6.0	-	mA
Output Voltage Low	VOL	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V, IOL = 50μA	+25°C	-	0.1	V
Output Voltage High	VOH	VCC = 4.5V or 5.5V, VIH = VCC/2, VIL = 0.8V, IOH = -50μA	+25°C	VCC -0.1	-	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±5	μA
Three-State Output Leakage Current	IOZ	Applied Voltage = 0V or VCC, VCC = 5.5V	+25°C	-	±50	μA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, (Note 3)	+25°C	-	-	-
Data to Output	TPHL, TPLH	VCC = 4.5V	+25°C	2	22	ns
Enable to Output	TPZL	VCC = 4.5V	+25°C	2	26	ns
	TPZH	VCC = 4.5V	+25°C	2	21	ns
Disable to Output	TPLZ	VCC = 4.5V	+25°C	2	23	ns
	TPHZ	VCC = 4.5V	+25°C	2	22	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns, VIL = GND, VIH = 3V.
3. For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

PARAMETER	GROUP B SUBGROUP	DELTA LIMIT
ICC	5	12μA
IOL/IOH	5	-15% of 0 Hour
IOZL/IOZH	5	±200nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test I (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test II (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test III (Postburn-In)		100%/5004	1, 7, 9	
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 7, 9	

NOTE: 1. Alternated Group A Inspection in accordance with Method 5005 of MIL-STD-883 may be exercised.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE: 1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

OPEN	GROUND	1/2 VCC = 3V ± 0.5V	VCC = 5V ± 0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN I TEST CONNECTIONS (Note 1)					
11 - 18	1 - 10, 19	-	20	-	-
STATIC BURN-IN II TEST CONNECTIONS (Note 1)					
11 - 18	10	-	1 - 9, 19, 20	-	-
DYNAMIC BURN-IN TEST CONNECTIONS (Note 2)					
-	10	11 - 18	20	1, 19	2 - 9

NOTES:

1. Each pin except VCC and GND will have a resistor of 10kΩ ± 5% for static burn-in
2. Each pin except VCC and GND will have a resistor of 680Ω ± 5% for dynamic burn-in

TABLE 9. IRRADIATION TEST CONNECTIONS

OPEN	GROUND	VCC = 5V ± 0.5V
11 - 18	10	1 - 9, 19, 20

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing.
Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Harris Space Level Product Flow - 'MS'

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 24 hrs. min., +125°C min., Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% Static Burn-In 2, Condition A or B, 24 hrs. min., +125°C min., Method 1015

100% Interim Electrical Test 2 (T2)

100% Delta Calculation (T0-T2)

100% PDA 1, Method 5004 (Notes 1and 2)

100% Dynamic Burn-In, Condition D, 240 hrs., +125°C or Equivalent, Method 1015

100% Interim Electrical Test 3 (T3)

100% Delta Calculation (T0-T3)

100% PDA 2, Method 5004 (Note 2)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic, Method 2012 (Note 3)

100% External Visual, Method 2009

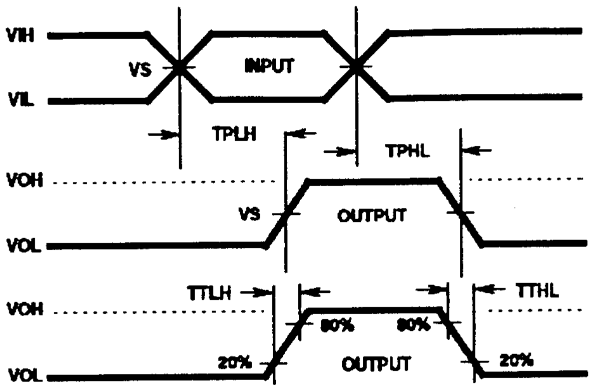
Sample - Group A, Method 5005 (Note 4)

100% Data Package Generation (Note 5)

NOTES:

1. Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
2. Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Data Package Contents:
   - Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
   - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
   - X-Ray report and film. Includes penetrometer measurements.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Lot Serial Number Sheet (Good units serial number and lot number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

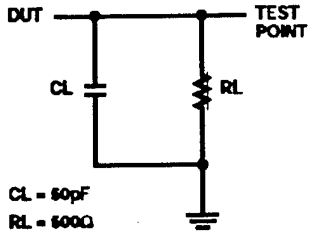
AC Timing Diagrams



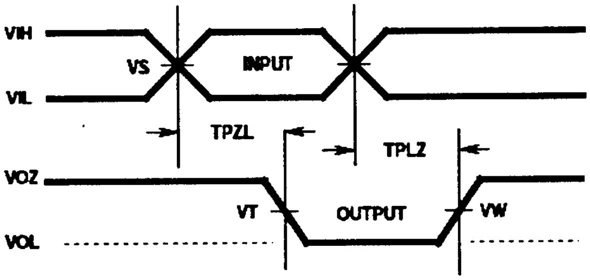
AC VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VIL	0	V
VSS	0	V

AC Load Circuit



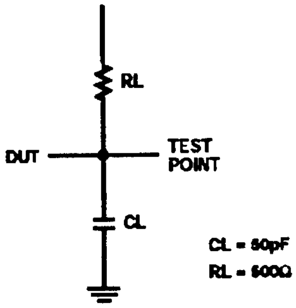
Three-State Low Timing Diagrams



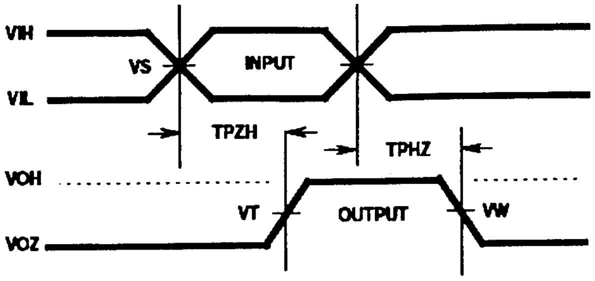
THREE-STATE LOW VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	0.90	V
GND	0	V

Three-State Low Load Circuit



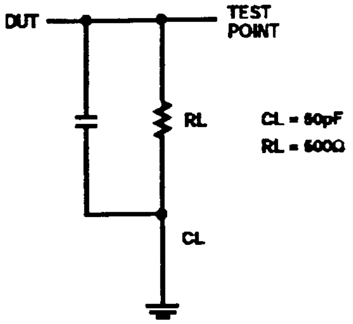
Three-State High Timing Diagrams



THREE-STATE HIGH VOLTAGE LEVELS

PARAMETER	HCTS	UNITS
VCC	4.50	V
VIH	3.00	V
VS	1.30	V
VT	1.30	V
VW	3.60	V
GND	0	V

Three-State High Load Circuit



Die Characteristics

DIE DIMENSIONS:
101 x 85 mils

METALLIZATION:
Type: SiAl
Metal Thickness: 11kÅ ± 1kÅ

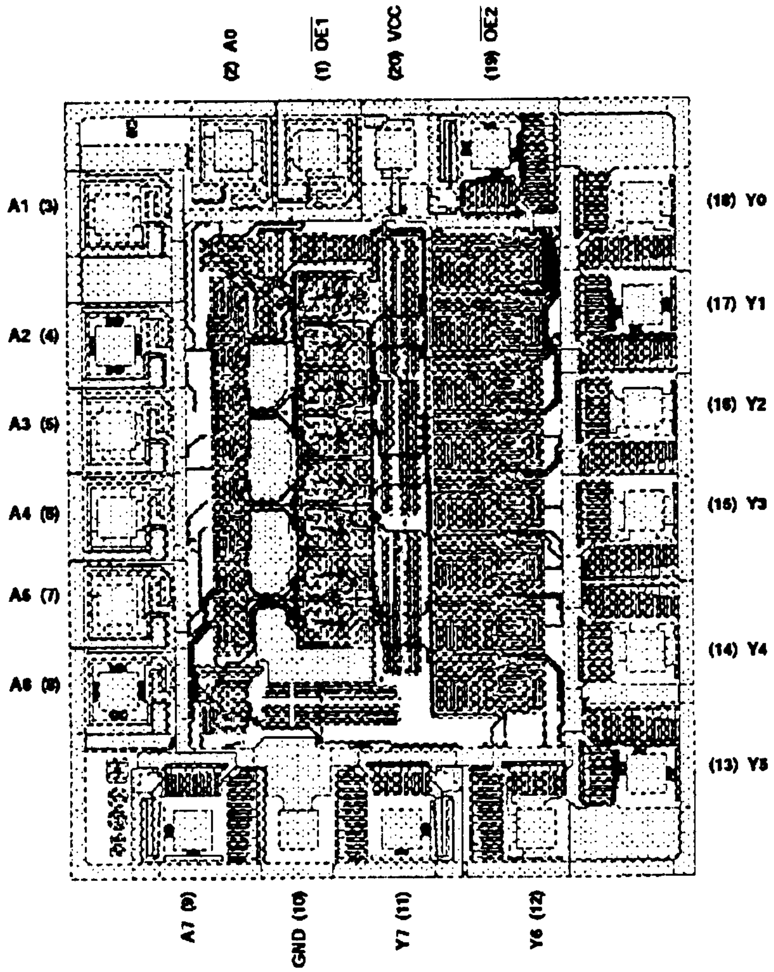
GLASSIVATION:
Type: SiO_2
Thickness: 13kÅ ± 2.6kÅ

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:
100μm x 100μm
4 mils x 4 mils

Metallization Mask Layout

HCTS541MS



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCTS541 is TA14456A.

HARRIS
SEMICONDUCTOR

HS-82C85RH

Radiation Hardened CMOS Static Clock Controller/Generator

August 1995

Features

- Radiation Hardened
  - Total Dose > 10^5 RAD (Si)
  - Transient Upset > 10^8 RAD (Si)/s
  - Latch Up Free EPI-CMOS
- Very Low Power Consumption
- Pin Compatible with NMOS 8285 and Harris 82C85
- Generates System Clocks for Microprocessors and Peripherals
- Complete Control Over System Clock Operation for Very Low System Power
  - Stop-Oscillator
  - Stop-Clock
  - Low Frequency (Slo) Mode
  - Full Speed Operation
- DC to 15MHz Operation (DC to 5MHz System Clock)
- Generates Both 50% and 33% Duty Cycle Clocks (Synchronized)
- Uses Either Parallel Mode Crystal Circuit or External Frequency Source
- Hardened Field, Self-Aligned, Junction Isolated CMOS Process
- Single 5V Supply
- Military Temperature Range -55°C to +125°C

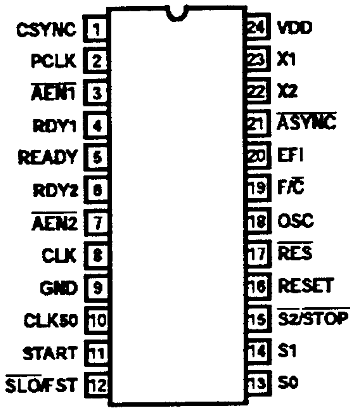
Description

The Harris HS-82C85RH is a high performance, radiation hardened CMOS Clock Controller/Generator designed to support systems utilizing radiation hardened static CMOS microprocessors such as the HS-80C86RH. The HS-82C85RH contains a crystal controlled oscillator, reset pulse conditioning, halt/restart logic, and divide-by-256 circuitry. These features provide the means to stop the system clock, stop the clock oscillator, or run the system at a low frequency (CLK/256), enhancing control of static system power dissipation and allowing system shut-down during periods of external stress.

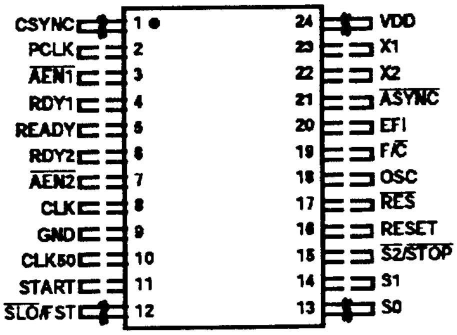
Static CMOS circuit design insures low operating power and permits operation with an external frequency source from DC to 15MHz. Crystal controlled operation to 15MHz is guaranteed with the use of a parallel, fundamental mode crystal and two small load capacitors. Outputs are guaranteed compatible with both CMOS and TTL specifications. The Harris hardened field CMOS process results in performance equal to or greater than existing radiation resistant products at a fraction of the power.

Pinouts

24 LEAD CERAMIC DUAL-IN-LINE
METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T24
TOP VIEW



24 LEAD CERAMIC METAL SEAL
FLATPACK PACKAGE (FLATPACK)
MIL-STD-1835 CDFP4-F24
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HS1-82C85RH-Q	-55°C to +125°C	24 Lead SBDIP
HS1-82C85RH-8	-55°C to +125°C	24 Lead SBDIP
HS1-82C85RH/Sample	+25°C	24 Lead SBDIP
HS9-82C85RH/Proto	-55°C to +125°C	24 Lead Ceramic Flatpack
HS9-82C85RH-Q	-55°C to +125°C	24 Lead Ceramic Flatpack
HS9-82C85RH-8	-55°C to +125°C	24 Lead Ceramic Flatpack
HS9-82C85RH/Sample	+25°C	24 Lead Ceramic Flatpack

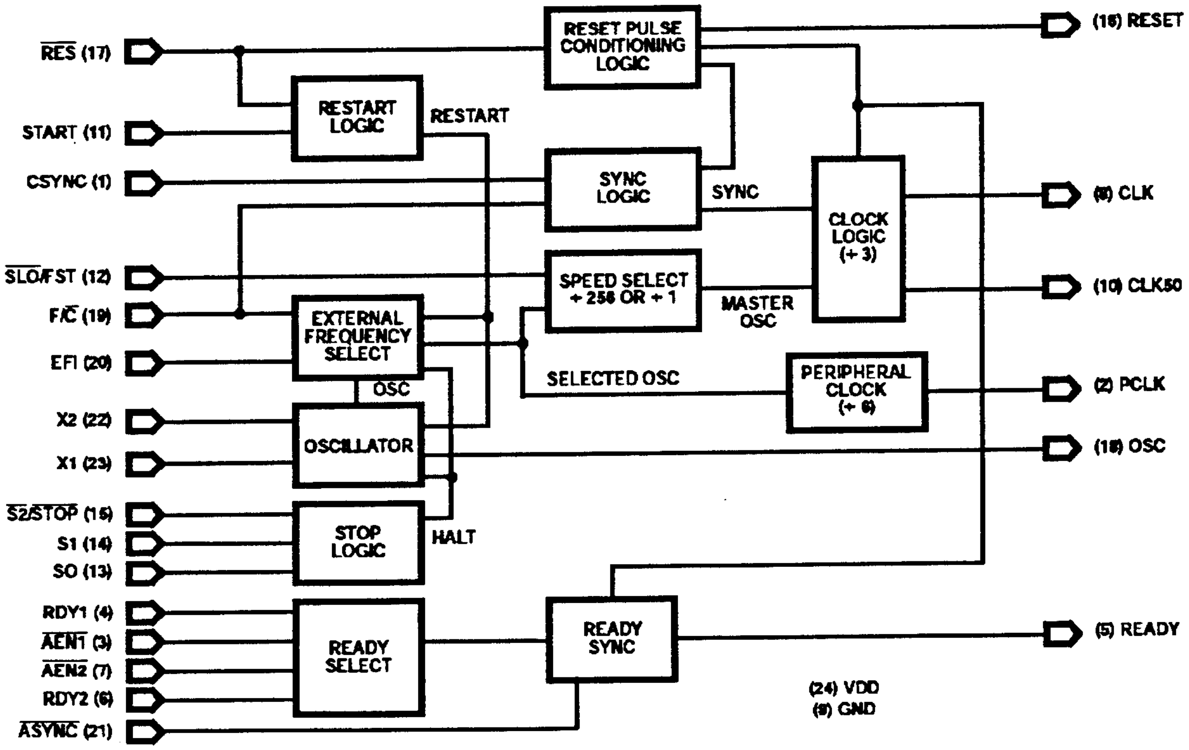
Pin Description

PIN	PIN NUMBER	TYPE	DESCRIPTION
X1 X2	23 22	I O	CRYSTAL CONNECTIONS: X1 and X2 are the crystal oscillator connections. The crystal frequency must be three times the maximum desired processor clock frequency. X1 is the oscillator circuit input and X2 is the output of the oscillator circuit.
EFI	20	I	EXTERNAL FREQUENCY IN: When F/$\overline{\text{C}}$ is HIGH, CLK is generated from the EFI input signal. This input signal should be a square wave with a frequency of three times the maximum desired CLK output frequency.
F/$\overline{\text{C}}$	19	I	FREQUENCY/CRYSTAL SELECT: F/$\overline{\text{C}}$ selects either the crystal oscillator or the EFI input as the main frequency source. When F/$\overline{\text{C}}$ is LOW, the HS-82C85RH clocks are derived from the crystal oscillator circuit. When F/$\overline{\text{C}}$ is HIGH, CLK is generated from the EFI input. F/$\overline{\text{C}}$ cannot be dynamically switched during normal operation.
START	11	I	A low-to-high transition on START will restart the CLK, CLK50 and PCLK outputs after the appropriate restart sequence is completed. When in the crystal mode (F/$\overline{\text{C}}$ LOW) with the oscillator stopped, the oscillator will be restarted when a Start command is received. The CLK, CLK50 and PCLK outputs will start after the oscillator input signal (X1) reaches the Schmitt trigger input threshold and an 8K internal counter reaches terminal count. If F/$\overline{\text{C}}$ is HIGH (EFI mode), CLK, CLK50 and PCLK will restart within 3 EFI cycles after START is recognized. The HS-82C85RH will restart in the same mode ($\overline{\text{SLO}}$/FST) in which it stopped. A high level on START disables the STOP mode.
S0 S1 S2/$\overline{\text{STOP}}$	13 14 15	I I I	S2/$\overline{\text{STOP}}$, S1, S0 are used to stop the HS-82C85RH clock outputs (CLK, CLK50, PCLK) and are sampled by the rising edge of CLK. CLK, CLK50 and PCLK are stopped by S2/$\overline{\text{STOP}}$,S1, S0 being in the LHH state on the low-to-high transition of CLK. This LHH state must follow a passive HHH state occurring on the previous low-to-high CLK transition. CLK and CLK50 stop in the high state. PCLK stops in it's current state (high or low). When in the crystal mode (F/$\overline{\text{C}}$) low and a STOP command is issued, the HS-82C85RH oscillator will stop along with the CLK, CLK50 and PCLK outputs. When in the EFI mode, only the CLK, CLK50 and PCLK outputs will be halted. The oscillator circuit if operational, will continue to run. The oscillator and/or clock is restarted by the START input signal going true (HIGH) or the reset input ($\overline{\text{RES}}$) going low.
$\overline{\text{SLO}}$/FST	12	I	$\overline{\text{SLO}}$/FST is a level-triggered input. When HIGH, the CLK and CLK50 outputs run at the maximum frequency (crystal or EFI frequency divided by 3). When LOW, CLK and CLK50 frequencies are equal to the crystal or EFI frequency divided by 768. $\overline{\text{SLO}}$/FST mode changes are internally synchronized to eliminate glitches on the CLK and CLK50. START and STOP control of the oscillator or EFI is available in either the SLOW or FAST frequency modes. The $\overline{\text{SLO}}$/FST input must be held LOW for at least 195 OSC/EFI clock cycles before it will be recognized. This eliminates unwanted frequency changes which could be caused by glitches or noise transients. The $\overline{\text{SLO}}$/FST input must be held HIGH for at least 6 OSC/EFI clock pulses to guarantee a transition to FAST mode operation.
CLK	8	O	PROCESSOR CLOCK: CLK is the clock output used by the HS-80C86RH processor and other peripheral devices. When $\overline{\text{SLO}}$/FST is high, CLK has an output frequency which is equal to the crystal or EFI input frequency divided by three. When $\overline{\text{SLO}}$/FST is low, CLK has an output frequency which is equal to the crystal or EFI input frequency divide by 768. CLK has a 33% duty cycle.
CLK50	10	O	50% DUTY CYCLE CLOCK: CLK50 is an auxiliary clock with a 50% duty cycle and is synchronized to the falling edge of CLK. When $\overline{\text{SLO}}$/FST is high, CLK50 has an output frequency which is equal to the crystal or EFI input frequency divided by 3. When $\overline{\text{SLO}}$/FST is low, CLK50 has an output frequency equal to the crystal or EFI input frequency divided by 768.
PCLK	2	O	PERIPHERAL CLOCK: PCLK is a peripheral clock signal whose output frequency is equal to the crystal or EFI input frequency divided by six and has a 50% duty cycle. PCLK frequency is unaffected by the state of the $\overline{\text{SLO}}$/FST input.
OSC	18	O	OSCILLATOR OUTPUT: OSC is the output of the internal oscillator circuitry. Its frequency is equal to that of the crystal oscillator circuit. OSC is unaffected by the state of the $\overline{\text{SLO}}$/FST input. When the HS-82C85RH is in the crystal mode (F/$\overline{\text{C}}$ LOW) and a STOP command is issued, the OSC output will stop in the HIGH state. When the HS-82C85RH is in the EFI mode (F/$\overline{\text{C}}$ HIGH), the oscillator (if operational) will continue to run when a STOP command is issued and OSC remains active.

Pin Description (Continued)

PIN	PIN NUMBER	TYPE	DESCRIPTION
$\overline{\text{RES}}$	17	I	RESET IN: $\overline{\text{RES}}$ is an active LOW signal which is used to generate RESET. The HS-82C85RH provides a Schmitt trigger input so that an RC connection can be used to establish the power-up reset of proper duration. $\overline{\text{RES}}$ starts crystal oscillator operation.
RESET	16	O	RESET: RESET is an active HIGH signal which is used to reset the HS-80C86RH processor. Its timing characteristics are determined by $\overline{\text{RES}}$. RESET is guaranteed to be HIGH for a minimum of 16 CLK pulses after the rising edge of $\overline{\text{RES}}$.
CSYNC	1	I	CLOCK SYNCHRONIZATION: CSYNC is an active HIGH signal which allows multiple HS-82C85RHs to be synchronized to provide multiple in-phase clock signals. When CSYNC is HIGH, the internal counters are reset and force CLK, CLK50 and PCLK into a HIGH state. When CSYNC is LOW, the internal counters are allowed to count and the CLK,CLK50 and PCLK outputs are active. CSYNC must be externally synchronized to EFI.
$\overline{\text{AEN1}}$ $\overline{\text{AEN2}}$	3 7	I I	ADDRESS ENABLE: $\overline{\text{AEN}}$ is an active LOW signal. $\overline{\text{AEN}}$ serves to qualify its respective Bus Ready Signal (RDY1 or RDY2). $\overline{\text{AEN1}}$ validates RDY1 while $\overline{\text{AEN2}}$ validates RDY2. Two $\overline{\text{AEN}}$ signal inputs are useful in system configurations which permit the processor to access two Multi-Master System Buses.
RDY1 RDY2	4 6	I I	BUS READY: (Transfer Complete). RDY is an active HIGH signal which is an indication from a device located on the system data bus that data has been received, or is available. RDY1 is qualified by $\overline{\text{AEN1}}$ while RDY2 is qualified by $\overline{\text{AEN2}}$.
$\overline{\text{ASYNC}}$	21	I	READY SYNCHRONIZATION SELECT: $\overline{\text{ASYNC}}$ is an input which defines the synchronization mode of the READY logic. When $\overline{\text{ASYNC}}$ is LOW, two stages of READY synchronization are provided. When $\overline{\text{ASYNC}}$ is left open or HIGH a single stage of READY synchronization is provided.
READY	5	O	READY: READY is an active HIGH signal which is used to inform the HS-80C86RH that it may conclude a pending data transfer.
GND	9	I	Ground
VDD	24	I	+5V power supply

Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . +6.5V
Input, Output or I/O Voltage . . . . VSS-0.3V to VDD+0.3V
Storage Temperature Range . . . . -65°C to +150°C
Junction Temperature . . . . +175°C
Lead Temperature (Soldering 10s) . . . . +300°C
Typical Derating Factor . . . . 5.33mA/MHz Increase in IDDOP
ESD Classification . . . . Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	52°C/W	12°C/W
Ceramic Flatpack Package	70°C/W	10°C/W

Maximum Package Power Dissipation at +125°C Ambient
SBDIP Package 0.96W
Ceramic Flatpack Package 0.71W

If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate:
SBDIP Package 19.2mW/C
Ceramic Flatpack Package 14.3mW/C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . +4.5V to +5.5V
Operating Temperature Range . . . . -55°C to +125°C
RESET Input High Voltage . . . . 3.5V to VDD
Input Low Voltage . . . . 0V to +0.8V
Input High Voltage . . . . 3.5V to VDD

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
CLK or CLK50 Output High Voltage	VOH	VDD = 4.5V, IO = -5.0mA, VIN = 0V or 4.5V	1, 2, 3	-55°C, +25°C, +125°C	VDD -0.4	-	V
Output High Voltage	VOH	VDD = 4.5V, IO = -2.5mA, VIN = 0V or 4.5V	1, 2, 3	-55°C, +25°C, +125°C	VDD -0.4	-	V
Output Low Voltage	VOL	VDD = 4.5V, IO = 5.0mA, VIN = 0V or 4.5V	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
Input Leakage Current	IIL or IIH	VDD = 5.5V, VIN = 0V or 5.5V, Input Pins except 11 to 15, 21, 23	1, 2, 3	-55°C, +25°C, +125°C	-1.0	1.0	µA
Bus Hold High Leakage Current (Note 1)	IBHH	VDD = 4.5V, 5.5V, VIN = 3.0V, Pins: 11 to 15, 21	1, 2, 3	-55°C, +25°C, +125°C	-200	-20	µA
Standby Power Supply Current	IDDSB	VDD = 5.5V, VIN = GND or VDD, IO = 0mA	1, 2, 3	-55°C, +25°C, +125°C	-	100	µA
Operating Power Supply Current	IDDOP	VDD = 5.5V, VIN = GND or VDD, IO = 0mA, Crystal Frequency = 15MHz	1, 2, 3	-55°C, +25°C, +125°C	-	80	mA
Functional Tests	FT	VDD = 4.5V and 5.5V, VIN = GND or VDD, f = 1MHz	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-
Noise Immunity Functional Test	FN	VDD = 5.5V, VIN = GND or 3.5V and VDD = 4.5V, VIN = 0.8V or VDD	7, 8A, 8B	-55°C, +25°C, +125°C	-	-	-

NOTE:

1. IBHH should be measured after raising VIN to VDD and then lowering to 3.0V

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 4.5V, T_A = -55°C to +125°C

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
TIMING REQUIREMENTS							
External Frequency High Time	TEHEL	90% - 90% VIN	9, 10, 11	-55°C, +25°C, +125°C	25	-	ns
External Frequency Low Time	TELEH	10% - 10% VIN	9, 10, 11	-55°C, +25°C, +125°C	25	-	ns
EFI or Crystal Period	TELEL		9, 10, 11	-55°C, +25°C, +125°C	65	-	ns
External Frequency Input Duty Cycle	TEFIDC		9, 10, 11	-55°C, +25°C, +125°C	45	55	%
Crystal Frequency	FX		9, 10, 11	-55°C, +25°C, +125°C	2.4	15	MHz
RDY1, RDY2 Active Setup to CLK	TR1VCL	$\overline{\text{ASYNC}}$ = High	9, 10, 11	-55°C, +25°C, +125°C	55	-	ns
RDY1, RDY2 Active Setup to CLK	TR1VCH	$\overline{\text{ASYNC}}$ = Low	9, 10, 11	-55°C, +25°C, +125°C	55	-	ns
RDY1, RDY2 Inactive Setup to CLK	TR1VCL		9, 10, 11	-55°C, +25°C, +125°C	55	-	ns
RDY1, RDY2 Hold to CLK	TCLR1X		9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
$\overline{\text{ASYNC}}$ Setup to CLK	TAYVCL		9, 10, 11	-55°C, +25°C, +125°C	84	-	ns
$\overline{\text{ASYNC}}$ Hold to CLK	TCLAYX		9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
$\overline{\text{AEN1}}$, $\overline{\text{AEN2}}$ Setup to RDY1, RDY2	TA1VR1V		9, 10, 11	-55°C, +25°C, +125°C	25	-	ns
$\overline{\text{AEN1}}$, $\overline{\text{AEN2}}$ Hold to CLK	TCLA1X		9, 10, 11	-55°C, +25°C, +125°C	0	-	ns
CSYNC Setup to EFI	TYHEH		9, 10, 11	-55°C, +25°C, +125°C	17	-	ns
CSYNC Hold to EFI	TEHYL		9, 10, 11	-55°C, +25°C, +125°C	17	-	ns
CSYNC Pulse Width	TYHYL		9, 10, 11	-55°C, +25°C, +125°C	2TELEL	-	ns
$\overline{\text{RES}}$ Setup to CLK	TI1HCL	Note 3	9, 10, 11	-55°C, +25°C, +125°C	105	-	ns
S0, S1, S2/$\overline{\text{STOP}}$ Setup to CLK	TSVCH		9, 10, 11	-55°C, +25°C, +125°C	55	-	ns
S0, S1, S2/$\overline{\text{STOP}}$ Hold to CLK	TCHSX		9, 10, 11	-55°C, +25°C, +125°C	55	-	ns
$\overline{\text{RES}}$, START Setup to CLK	TRSVCH	Note 3	9, 10, 11	-55°C, +25°C, +125°C	105	-	ns
$\overline{\text{RES}}$ (Low) or START (High) Pulse Width	TSHSL		9, 10, 11	-55°C, +25°C, +125°C	2/3 TCLCL	-	ns
$\overline{\text{SLO}}$/FST Setup to PCLK	TSFPC	Note 3	9, 10, 11	-55°C, +25°C, +125°C	TEHEL+170	-	ns
TIMING RESPONSES							
CLK/CLK50 Cycle Period	TCLCL		9, 10, 11	-55°C, +25°C, +125°C	200	-	ns
CLK HIGH Time	TCHCL		9, 10, 11	-55°C, +25°C, +125°C	(1/3 TCLCL) +3	-	ns
CLK LOW	TCLCH		9, 10, 11	-55°C, +25°C, +125°C	(2/3 TCLCL) -15	-	ns
CLK50 HIGH Time	T5CHCL		9, 10, 11	-55°C, +25°C, +125°C	(1/2 TCLCL) -7.5	-	ns
CLK50 LOW Time	T5CLCH		9, 10, 11	-55°C, +25°C, +125°C	(1/2 TCLCL) -7.5	-	ns
PCLK HIGH Time	TPHPL		9, 10, 11	-55°C, +25°C, +125°C	TCLCL-20	-	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS VDD = 4.5V, T_A = -55°C to +125°C (Continued)

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
PCLK LOW Time	TPLPH		9, 10, 11	-55°C, +25°C, +125°C	TCLCL-20	-	ns
Ready Inactive to CLK	TRYLCL	Note 4	9, 10, 11	-55°C, +25°C, +125°C	-8	-	ns
Ready Active to CLK	TRYHCH	Note 3	9, 10, 11	-55°C, +25°C, +125°C	2/3(TCLCL) -15	-	ns
CLK to Reset Delay	TCLIL		9, 10, 11	-55°C, +25°C, +125°C	-	65	ns
CLK to PCLK HIGH Delay	TCLPH		9, 10, 11	-55°C, +25°C, +125°C	-	40	ns
CLK to PCLK LOW Delay	TCLPL		9, 10, 11	-55°C, +25°C, +125°C	-	40	ns
OSC to CLK HIGH Delay	TOHCH		9, 10, 11	-55°C, +25°C, +125°C	-5	60	ns
OSC to CLK LOW Delay	TOHCL		9, 10, 11	-55°C, +25°C, +125°C	2	70	ns
OSC LOW to CLK50 HIGH Delay	TOLCH		9, 10, 11	-55°C, +25°C, +125°C	-5	60	ns
CLK LOW to CLK50 LOW Skew	TCLC50L		9, 10, 11	-55°C, +25°C, +125°C	-	10	ns

NOTES:

1. ACs tested at worst case VDD, guaranteed over full operating range
2. Setup and hold necessary only to guarantee recognition at next clock
3. Applies only to T3, TW states
4. Applies only to T2 states
5. All timing delays are measured at 1.5V, unless otherwise noted
6. Timing measurements made with EFI duty cycle = 50%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Input Capacitance	CIN	VDD = Open, f = 1MHz, Note 2	T_A = +25°C	-	5	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz, Note 2	T_A = +25°C	-	15	pF
RESET Input Hysteresis	(+)VT - (-)VT	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	0.25	-	V
TIMING REQUIREMENTS						
$\overline{\text{RES}}$ or START Valid to CLK Low	TSTART	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	2TELEL +3	-	ns
$\overline{\text{STOP}}$ Command Valid to CLK High	TSTOP	VDD = 4.5V and 5.5V	-55°C < T_A < +125°C	TCLCL + TCLCH	3TCHCH +55	ns
TIMING RESPONSES						
CLK/CLK50 Rise Time	TCH1CH2	VDD = 4.5V and 5.5V, 1.0V to 3.5V	-55°C < T_A < +125°C	-	15	ns
CLK/CLK50 Fall Time	TCL1CL2	VDD = 4.5V and 5.5V, 3.5V to 1.0V	-55°C < T_A < +125°C	-	15	ns
Output Rise Time (Except CLK)	TOLOH	VDD = 4.5V and 5.5V, 0.8V to 2.0V	-55°C < T_A < +125°C	-	25	ns
Output Fall Time (Except CLK)	TOHOL	VDD = 4.5V and 5.5V, 2.0V to 0.8V	-55°C < T_A < +125°C	-	25	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	TEMPERATURE	LIMITS		UNITS
				MIN	MAX	
Start/Reset Valid to CLK Low	TOST	VDD = 4.5V and 5.5V (TYP) Note 3	$-55^{\circ}C < T_A < +125^{\circ}C$	-	3	ms
RESET Output Time High	TRST	VDD = 4.5V and 5.5V	$-55^{\circ}C < T_A < +125^{\circ}C$	16 (TCLCL)	-	ms

NOTES:

1. The parameters listed in table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
2. All measurements referenced to device ground.
3. Oscillator start-up time depends on several factors including crystal frequency, crystal manufacturer, capacitive load, temperature, power supply voltage, etc. This parameter is given for information only.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

See +25°C limits in Table 1 and Table 2 for Post RAD limits (Subgroups 1, 7, 9)

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	DELTA LIMITS
Static Current	IDDSB	±20μA
Input Leakage Current	IIL, IIH	±200nA
Low Level Output Voltage	VOL	±80mV
High Level Output Voltage	VOH	±150mV

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS			
		TESTED FOR -Q	RECORDED FOR -Q	TESTED FOR -8	RECORDED FOR -8
Initial Test	100% 5004	1, 7, 9	1 (Note 2)	1, 7, 9	
Interim Test	100% 5004	1, 7, 9, Δ	1, Δ (Note 2)	1, 7, 9	
PDA	100% 5004	1, 7, Δ	-	1, 7	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	-	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Subgroup B5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Δ	1, 2, 3, Δ (Note 2)	N/A	
Subgroup B6	Sample 5005	1, 7, 9	-	N/A	
Group C	Sample 5005	N/A	N/A	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group D	Sample 5005	1, 7, 9	-	1, 7, 9	
Group E, Subgroup 2	Sample 5005	1, 7, 9	-	1, 7, 9	

NOTES:

1. Alternate Group A testing in accordance with MIL-STD-883 method 5005 may be exercised.
2. Table 5 parameters only

Harris Space Level Product Flow -Q

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 2 Samples/Wafer, 0 Rejects

100% Die Attach

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

CSI and/or GSI PreCap (Note 6)

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 72 Hours Min, +125°C Min, Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% PDA 1, Method 5004 (Note 1)

100% Dynamic Burn-In, Condition D, 240 Hours, +125°C or Equivalent, Method 1015

100% Interim Electrical Test 2(T2)

100% Delta Calculation (T0-T2)

100% PDA 2, Method 5004 (Note 1)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% Radiographic (X-Ray), Method 2012 (Note 2)

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 3)

Sample - Group B, Method 5005 (Note 4)

Sample - Group D, Method 5005 (Notes 4 and 5)

100% Data Package Generation (Note 7)

CSI and/or GSI Final (Note 6)

NOTES:

1. Failures from subgroup 1, 7 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
2. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
3. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
4. Group B and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B Test, Group B Samples, Group D Test and Group D Samples.
5. Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group D Generic Data. Generic data is not guaranteed to be available and is therefore not available in all cases.
6. CSI and/or GSI inspections are optional and will not be performed unless required by theP.O. When required, the P.O. should include separate line items for CSI PreCap inspection, CSI final inspection, GSI PreCap inspection, and/or GSI final inspection.
7. Data Package Contents:
   - Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
   - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
   - X-Ray report and film. Includes penetrometer measurements.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Lot Serial Number Sheet (Good units serial number and lot number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - Group B and D attributes and/or Generic data is included when required by the P.O.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

Harris Space Level Product Flow -8

GAMMA Radiation Verification (Each Wafer) Method 1019, 2 Samples/Wafer, 0 Rejects

100% Die Attach

Periodic- Wire Bond Pull Monitor, Method 2011

Periodic- Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition B

CSI an/or GSI PreCap (Note 5)

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% External Visual

100% Initial Electrical Test

100% Dynamic Burn-In, Condition D, 160 Hours, +125°C or Equivalent, Method 1015

100% Interim Electrical Test

100% PDA, Method 5004 (Note 1)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 2)

Sample - Group B, Method 5005 (Note 3)

Sample - Group C, Method 5005 (Notes 3 and 4)

Sample - Group D, Method 5005 (Notes 3 and 4)

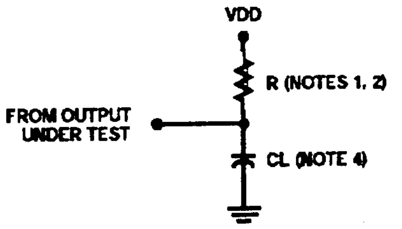
100% Data Package Generation (Note 6)

CSI and/or GSI Final (Note 5)

NOTES:

1. Failures from subgroup 1, 7 are used for calculating PDA. The maximum allowable PDA = 5%.
2. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
3. Group B, C and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B Test, Group C Test, Group C Samples, Group D Test and Group D Samples.
4. Group C and/or Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group C Generic Data and/or Group D Generic Data. Generic data is not guaranteed to be available and is therefore not available in all cases.
5. CSI and/or GSI inspections are optional and will not be performed unless required by theP.O. When required, the P.O. should include separate line items for CSI PreCap inspection, CSI final inspection, GSI PreCap inspection, and/or GSI final inspection.
6. Data Package Contents:
   - Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Group B, C and D attributes and/or Generic data is included when required by the P.O.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

AC Test Circuit



NOTES:

1. R = 370Ω at V = 2.25 for CLK and CLK50 outputs.
2. R = 494Ω at V = 2.87 for all other outputs.
3. CL = 50pF.
4. CL Includes probe and jig capacitance.

Waveforms

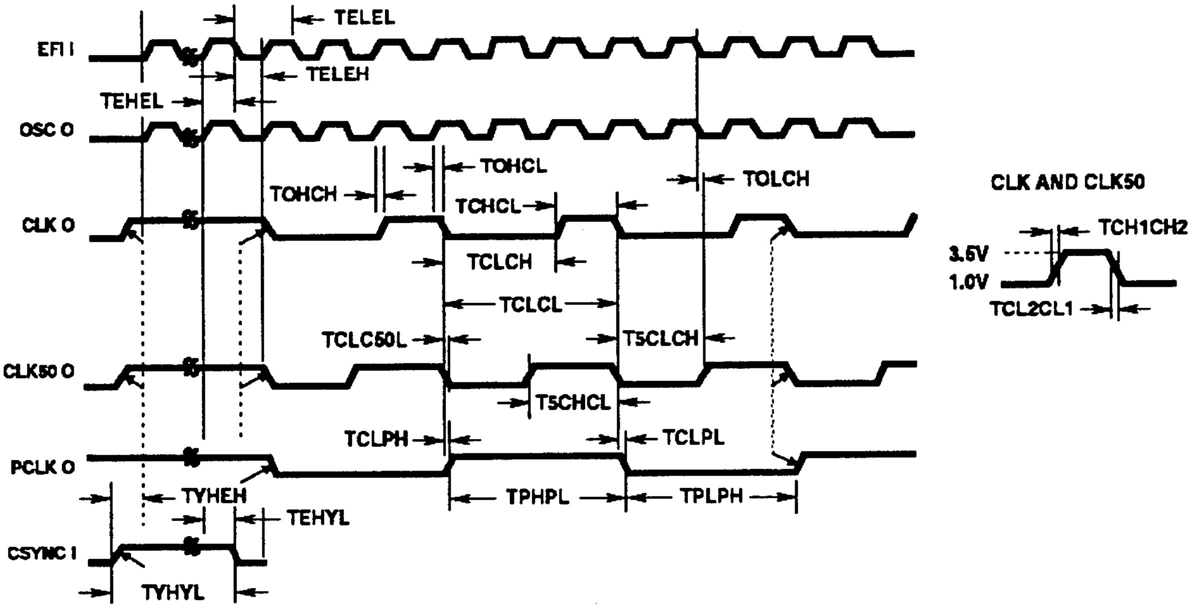


FIGURE 1. WAVEFORMS FOR CLOCKS

NOTE: All timing measurements are made at 1.5V, unless otherwise noted

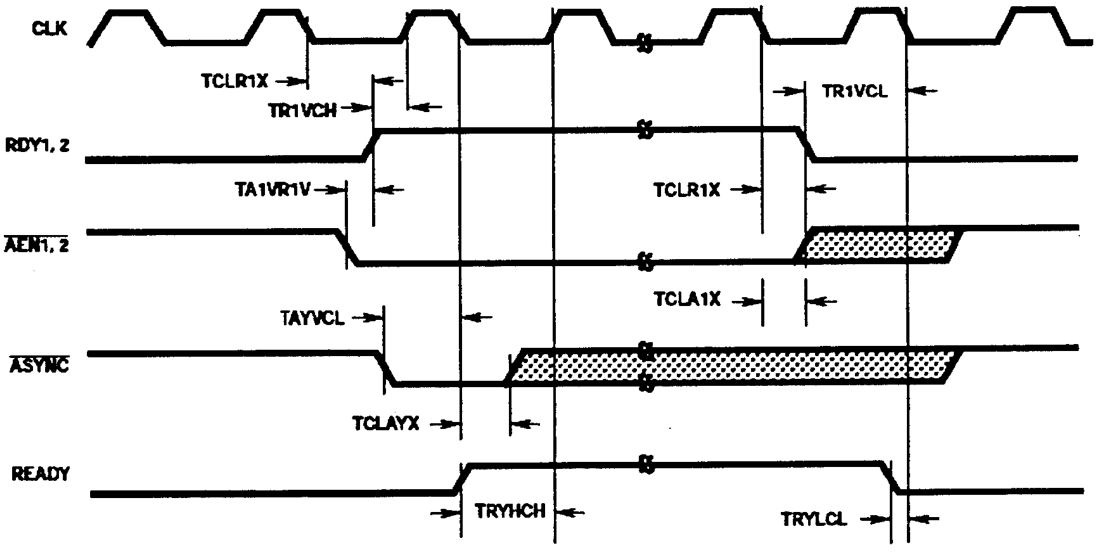


FIGURE 2. WAVEFORMS FOR READY SIGNALS (FOR ASYNCHRONOUS DEVICES)

Waveforms (Continued)

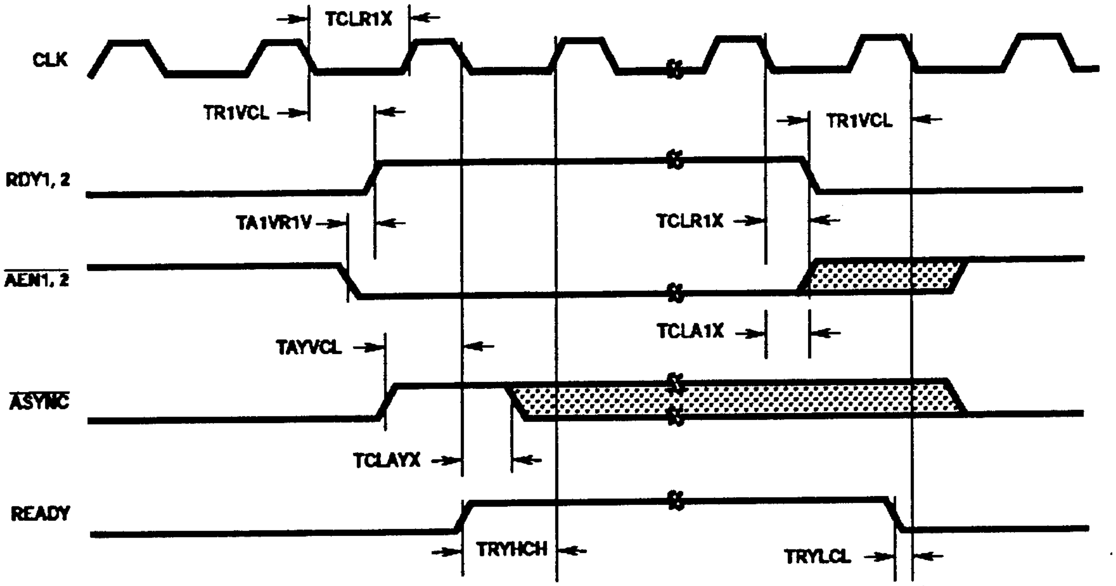


FIGURE 3. WAVEFORMS FOR READY SIGNALS (FOR SYNCHRONOUS DEVICES)

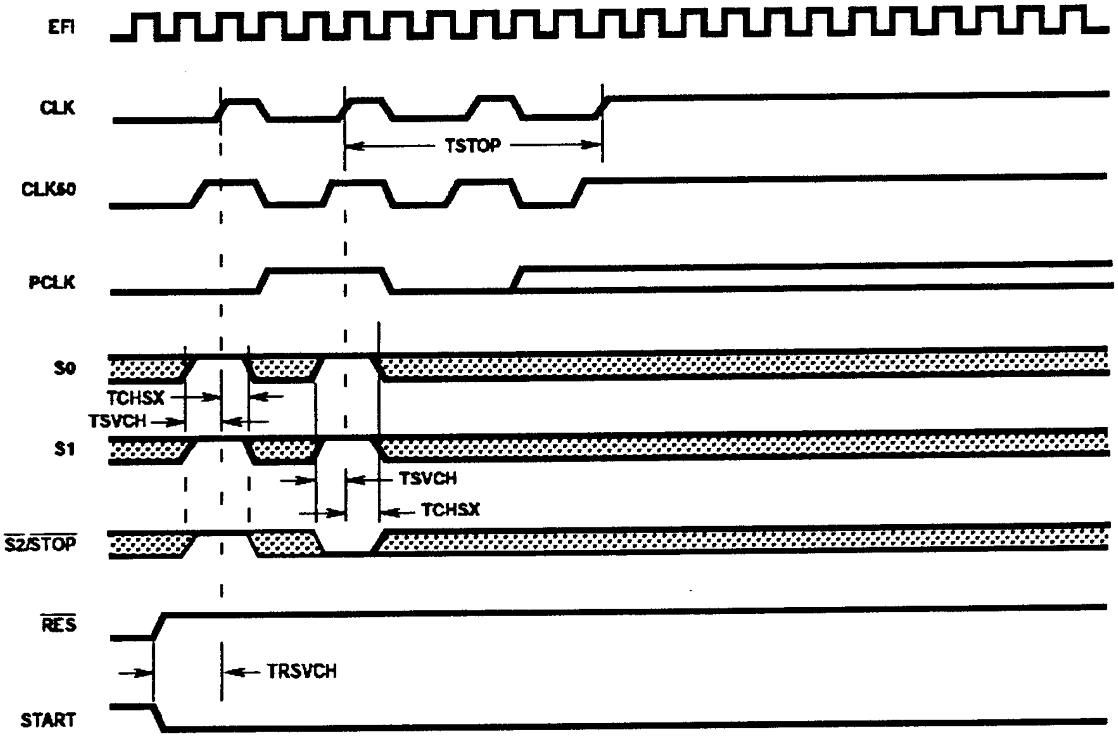


FIGURE 4. CLOCK STOP ($F/\overline{C}$ HIGH OR $F/\overline{C}$ LOW)

Waveforms (Continued)

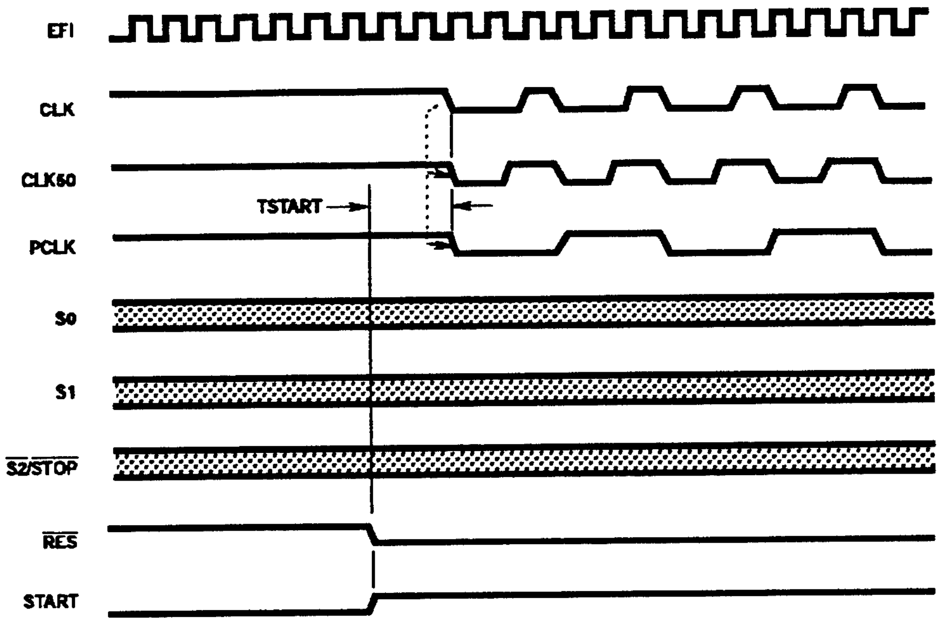


FIGURE 5. CLOCK START ($F/\overline{C}$ HIGH)

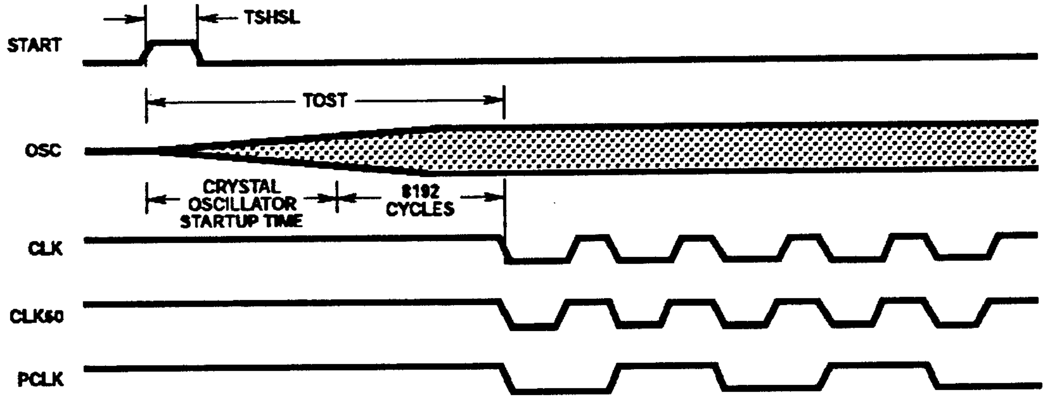


FIGURE 6. CLOCK START ($F/\overline{C}$ LOW)

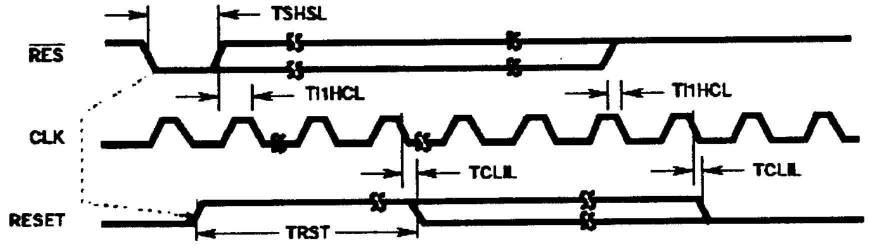


FIGURE 7. RESET TIMING (CLK RUNNING WITH $F/\overline{C}$ LOW - OSC MODE; CLK RUNNING - OR STOPPED WITH $F/\overline{C}$ HIGH EFI MODE)

Waveforms (Continued)

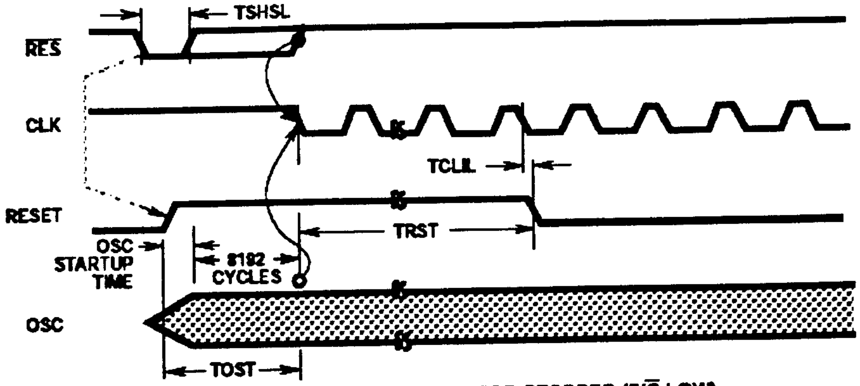


FIGURE 8. RESET TIMING OSCILLATOR STOPPED (F/$\overline{C}$ LOW)

NOTE: CLK, CLK50, PCLK remain in the high state until $\overline{RES}$ goes high and 8192 valid oscillator cycles have been registered by the HS-82C85RH internal counter TOST time period). After $\overline{RES}$ goes high and CLK, CLK50, PCLK become active, the RESET output will remain high for a minimum of 16 CLK cycles (TRST).

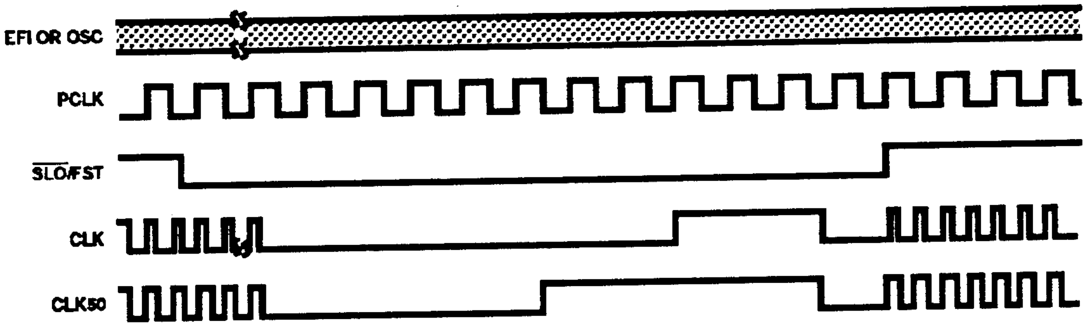


FIGURE 9. SLO/FST TIMING OVERVIEW

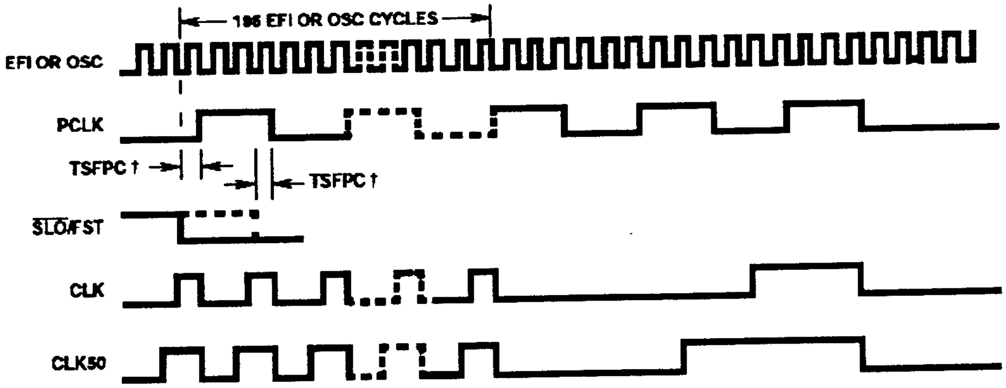


FIGURE 10. FAST TO SLOW CLOCK MODE TRANSITION

Waveforms (Continued)

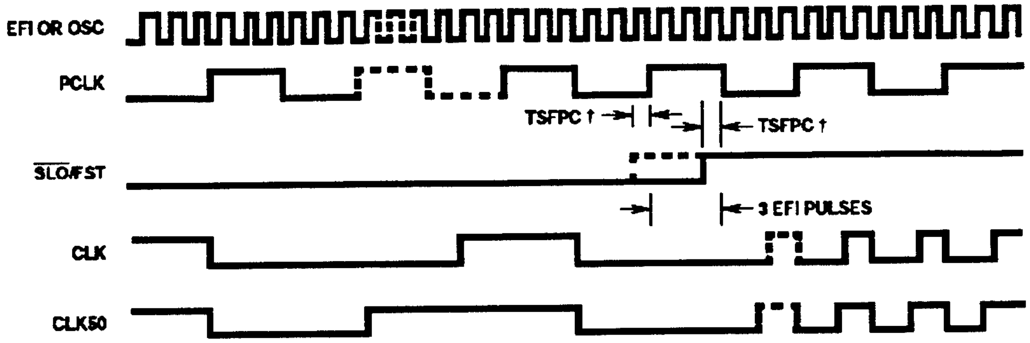


FIGURE 11. SLOW TO FAST CLOCK MODE TRANSITION

† If TSFPC is not met on one edge of PCLK, $\overline{\text{SLO}}$/FST will be recognized on the next edge of PCLK.

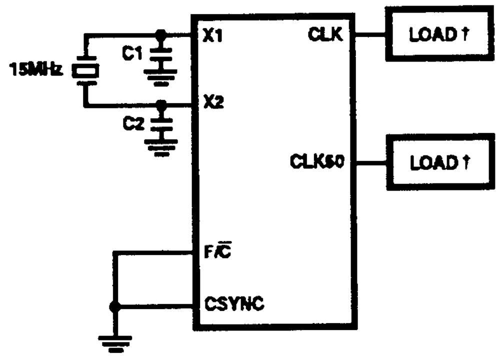


FIGURE 12. CLOCK HIGH AND LOW TIME (USING X1, X2)

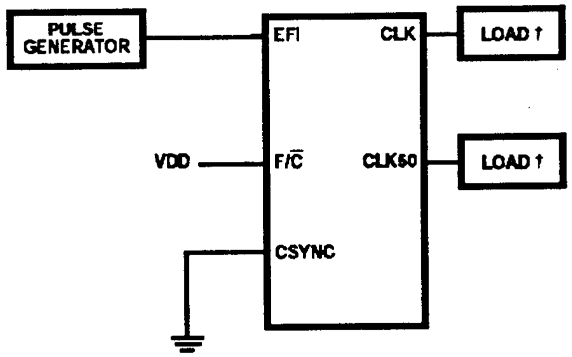


FIGURE 13. CLOCK HIGH AND LOW TIME (USING EFI)

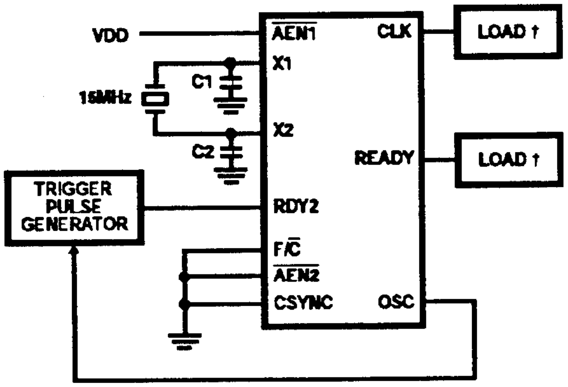


FIGURE 14. READY TO CLOCK (USING X1, X2)

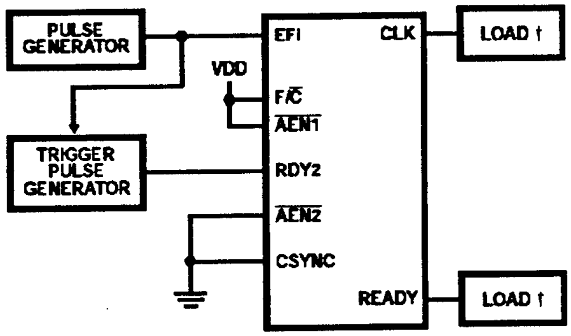
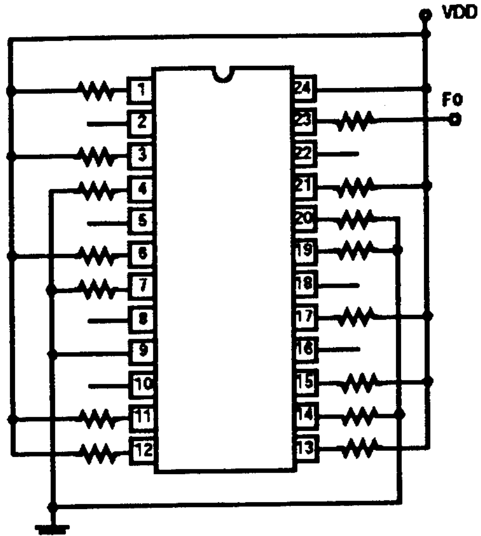


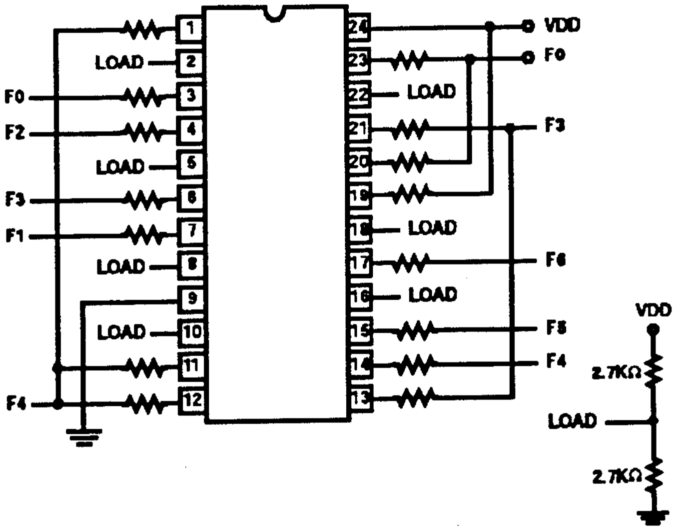
FIGURE 15. READY TO CLOCK (USING EFI)

† CL = 50pF

Burn-In Circuits



STATIC CONFIGURATION



DYNAMIC CONFIGURATION

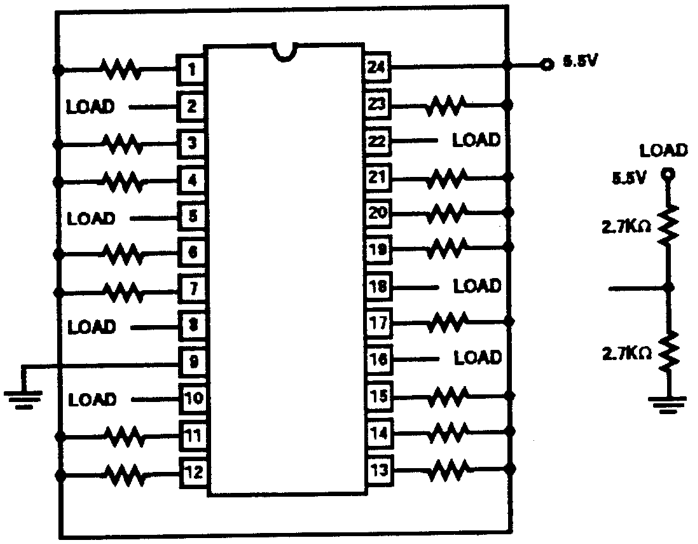
NOTES:

1. R = 10kΩ ± 10%
2. VDD = 6.0V ± 5%
3. T_A = +125°C Min
4. Package Code: SZ (24 Lead DIP)
5. F0 is 50% duty cycle square wave pulse burst. F0 is left low after pulse burst

NOTES:

1. R = 10kΩ ± 10%
2. VDD = 6.0V ± 5% (Burn-In); VDD = 5.5V ± 5% (Life Test)
3. T_A = +125°C Min
4. Package Code: SZ (24 Lead DIP)
5. F0 = 10kHz, 50% duty cycle
6. F1 = F0/2; F2 = F1/2; F3 = F2/2, F4 = F3/2; F5 = F4/2

Irradiation Circuit



NOTES:

1. R = 47kΩ ± 10%
2. Pins tied to VSS (0V): Pin 9
3. Pins with loads: 2, 5, 8, 10, 16, 18, 22
4. Pins tied to VDD: 1, 3, 4, 6, 7, 11 - 15, 17, 19 - 21, 23, 24
5. VDD = 5.5V ± 0.5V

Functional Description

The HS-82C85RH Static Clock Controller/Generator provides simple and complete control of static CMOS system operating modes. The HS-82C85RH can operate with either an external crystal or an external frequency source and can support full speed, slow, stop-clock and stop-oscillator operation. While it is directly compatible with the Harris HS-80C86RH CMOS 16-bit static microprocessor, the HS-82C85RH can also be used for general purpose system clock control.

Separate signals are provided on the HS-82C85RH for stop and start control of the crystal oscillator and clock outputs. A single control line determines fast (crystal/EFI frequency divided by 3) or slow (crystal/EFI frequency divided by 768) mode operation. A clock synchronization input is provided to allow the use of multiple HS-82C85RHs in the same system. The HS-82C85RH generates the proper HS-80C86RH reset pulse, and it also handles all data transfer timing by generating the HS-80C86RH ready signal.

Automatic maximum mode HS-80C86RH software HALT instruction decode logic is present to ease the design of software-based clock control systems and provides complete software control of STOP mode operation. Automatic minimum mode software HALT instruction decoding can be easily implemented with a single 74HC74 device. Restart logic insures valid clock start-up and complete synchronization of CLK, CLK50 and PCLK.

Static Operating Modes

The HS-82C85RH Static Clock Controller can be dynamically set to operate in any one of four modes at anyone time: FAST, SLOW, STOP-CLOCK and STOP-OSCILLATOR. Each mode has distinct power and performance characteristics which can be matched to the needs of a particular system at a specific time (See Table 1).

Keep in mind that a single system may require all of these operating modes at one time or another during normal operation. A design need not be limited to a single operating mode or a specific combination of modes. The appropriate operating mode can be matched to the power-performance level needed at a specific time or in a particular circumstance.

Reset Logic

The HS-82C85RH reset logic provides a Schmitt trigger input ($\overline{RES}$) and a synchronizing flip-flop to generate there set timing. The reset signal is synchronized to the falling edge of CLK. A simple RC network can be used to provide power-on reset by utilizing this function of the HS-82C85RH. When in the crystal oscillator ($F/\overline{C}$ = LOW) or the EFI ($F/\overline{C}$ = HIGH) mode, a LOW state on the $\overline{RES}$ input will set the RESET output to the HIGH state. It will also restart the oscillator circuit if it is in the idle state. The RESET output is guaranteed to stay in the HIGH state for a minimum of 16 CLK cycles after a low-to-high transition of the RES input.

An oscillator restart count sequence will not be disturbed by RESET if this count is already in progress. After the restart counter expires, the RESET output will stay HIGH at least for 16 periods of CLK before going LOW. RESET can be kept high beyond this time by a continuing low input on the $\overline{RES}$ input.

If F/C is low (crystal oscillator mode), a low state on $\overline{RES}$ starts the crystal oscillator circuit. The stopped outputs remain inactive, until the oscillator signal amplitude reaches the X1 Schmitt trigger input threshold voltage and 8192 cycles of the crystal oscillator output are counted by an internal counter. After this count is complete, the stopped outputs (CLK, CLK50, PCLK) start cleanly with the proper phase relationships.

This 8192 count requirement insures that the CLK, CLK50 and PCLK outputs will meet minimum clock requirements and will not be affected by unstable oscillator characteristics which may exist during the oscillator start-up sequence. This sequence is also followed when a START command is issued while the HS-82C85RH oscillator is stopped.

Oscillator/Clock Start Control

Once the oscillator is stopped (or committed to stop) or at power-on, the restart sequence is initiated by a HIGH state on START or LOW state on $\overline{RES}$. If $F/\overline{C}$ is HIGH, then restart occurs immediately after the START or $\overline{RES}$ input is synchronized internally. This insures that stopped outputs (CLK, PCLK, OSC and CLK50) start cleanly with the proper phase relationship.

TABLE 1. STATIC SYSTEM OPERATING MODE CHARACTERISTICS

OPERATING MODE	DESCRIPTION	POWER LEVEL	PERFORMANCE
Stop-Oscillator	All system clocks and main clock oscillator are stopped	Maximum savings	Slowest response due to oscillator restart time
Stop-Clock	System CPU and peripherals clocks stop but main clock oscillator continues to run at rated frequency	Reduced system power	Fast restart - no oscillator restart time
Slow	System CPU clocks are slowed while peripheral clock and main clock oscillator run at rated frequency	Power dissipation slightly higher than Stop-Clock	Continuous operation at low frequency
Fast	All clocks and oscillators run at rated frequency	Highest power	Fastest response

If F/$\overline{C}$ is low (crystal oscillator mode), a HIGH state on the START input or a low state on $\overline{RES}$ causes the crystal oscillator to be restarted. The stopped outputs remain stopped, until the oscillator signal amplitude reaches the X1 Schmitt trigger input threshold voltage and 8192 cycles of the crystal oscillator output are counted by an internal counter. After this count is complete, the stopped outputs (CLK, CLK50, PCLK) start cleanly with the proper phase relationships.

Typically, any input signal which meets the START Input timing requirements can be used to start the HS-82C85RH. In many cases, this would be the INT output from an HS-82C59A CMOS Priority Interrupt Controller (See Figure 16). This output, which is active high, can be connected to both the HS-82C85RH START pin and to the INTR input on the microprocessor.

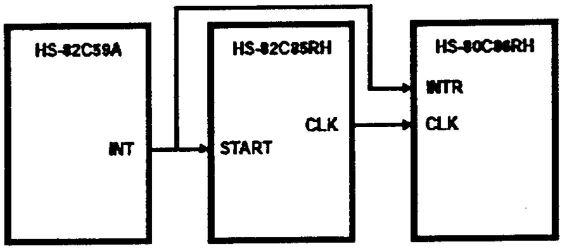


FIGURE 16. START CONTROL USING HS-82C59ARH INTERRUPT CONTROLLER

When the INT output becomes active (as a result of a "restart" IRQ or a system reset), the oscillator/clock circuit on the HS-82C85RH will restart. Upon completion of the appropriate restart sequence, the CLK signal to the CPU will become active. The CPU can then respond to the still-pending interrupt request.

Oscillator/Clock Stop Control

The S0, S1, and $\overline{S2/STOP}$ control lines determine when the HS-82C85RH clock outputs or oscillator will stop. These three lines are designed to connect directly to the MAXimum mode HS-80C86RH status lines as shown in Figure 17.

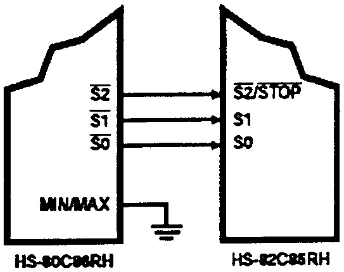


FIGURE 17. STOP CONTROL USING HS-80C86RH MAXIMUM MODE STATUS LINES

When used in this configuration, the HS-82C85RH will automatically recognize a software HALT command from the HS-80C86RH and stop the system clocks or oscillator. This allows complete software control of the STOP function.

If the HS-80C86RH is used in the MINimum mode, the HS-82C85RH can be controlled using the $\overline{S2/STOP}$ input (with S0 and S1 held high). This can be done using the circuit shown in Figure 18. Since the HS-80C86RH, when executing a halt instruction in minimum mode, issues a single ALE pulse with no corresponding bus signals ($\overline{DEN}$ remains high), the ALE pulse will be clocked through the 74HC74 and put the HS-82C85RH into stop mode.

The HS-82C85RH status inputs $\overline{S2/STOP}$, S1, S0 are sampled on the rising edge of CLK. The oscillator (F/$\overline{C}$ LOW only) and clock outputs are stopped by $\overline{S2/STOP}$, S1, S0 being in the LHH state on a low-to-high transition of CLK. This LHH state must follow a passive HHH state occurring on the previous low-to-high CLK transition. CLK and CLK50 will stop in the logic HIGH state after two additional complete cycles of CLK. PCLK stops in its current state (HIGH or LOW). This is true for both SLOW and FAST mode operation.

Stop-Oscillator Mode

When the HS-82C85RH is stopped while in the crystal mode (F/C LOW), the oscillator, in addition to all system clock signals (CLK, CLK50 and PCLK), are stopped. CLK and

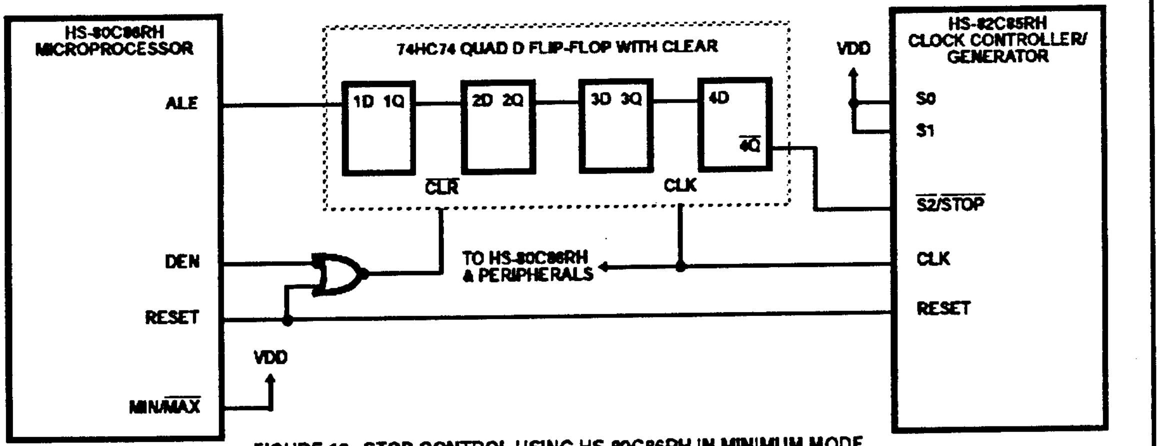


FIGURE 18. STOP CONTROL USING HS-80C86RH IN MINIMUM MODE

CLK50 stop in the high state. PCLK stops in its current state (high or low).

With the oscillator stopped, HS-82C85RH power drops to its lowest level. All clocks and oscillators are stopped. All devices in the system which are driven by the HS-82C85RH go into the lowest power standby mode.The HS-82C85RH also goes into standby and requires a power supply current of less than 100mA.

Stop-Clock Mode

When the HS-82C85RH is in the EFI mode (F/$\overline{\mathrm{C}}$ HIGH) and a STOP command is issued, all system clock signals (CLK, CLK50 and PCLK) are stopped. CLK and CLK50 stop in the high state. PCLK stops in its current state (high or low).

The HS-82C85RH can also provide its own EFI source simply by connecting the OSC output to the EFI input and pulling the F/$\overline{\mathrm{C}}$ input HIGH. This puts the HS-82C85RH into the External Frequency Mode using its own oscillator as an external source signal (See Figure 19). In this configuration, when the HS-82C85RH is stopped in the EFI mode, the oscillator continues to run. Only the clocks to the CPU and peripherals (CLK, CLK50 and PCLK) are stopped.

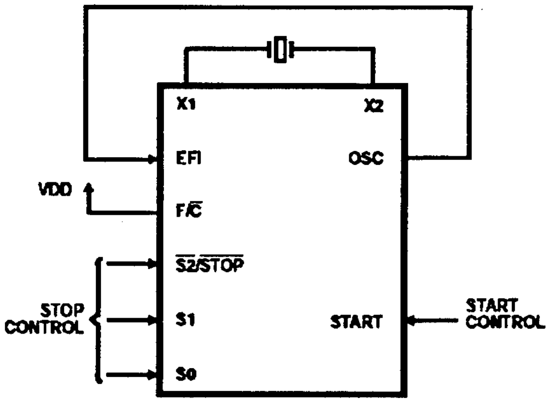


FIGURE 19. STOP-CLOCK MODE IN EFI MODE WITH OSCILLATOR AS FREQUENCY SOURCE

Clock Slow/Fast Operation

The $\overline{\mathrm{SLO}}$/FST input determines whether the CLK and CLK50 outputs run at full speed (crystal or EFI frequency divided by 3) or at slow speed (crystal or EFI frequency divided by 768) (See Figure 20). When in the SLOW mode,HS-82C85RH stop-clock and stop-oscillator functions operate in the same manner as in the FAST mode, and the frequency of PCLK is unaffected.

The SLOW mode allows the CPU and the system to operate at a reduced rate which, in turn, reduces system power. For example, the operating power for the HS-80C86RH CPU is 10mA/MHz of clock frequency. When the SLOW mode is used in a typical 5MHz system, CLK and CLK50 run at approximately 20kHz. At this reduced frequency, the average operating current of the CPU drops to 200mA. Adding the HS-80C86RH 500mA standby current brings the total current to 700mA.

While the CPU and peripherals run slower and the HS-82C85RH CLK and CLK50 outputs switch at a reduced frequency, the main HS-82C85RH oscillator is still running at the maximum frequency (determined by the crystal or EFI input frequency.) Since CMOS power is directly related to operating frequency, HS-82C85RH power supply current will typically be reduced by 25% - 35%.

Internal logic requires that the $\overline{\mathrm{SLO}}$/FST pin be held low for at least 195 oscillator or EFI clock pulses before the SLOW mode command is recognized. This requirement eliminates unwanted FAST-to-SLOW mode frequency changes which could be caused by glitches or noise spikes.

To guarantee FAST mode recognition, the $\overline{\mathrm{SLO}}$/FST pin must be held high for at least 3 OSC or EFI pulses. The HS-82C85RH will begin FAST mode operation on the next PCLK edge after FAST command recognition. Proper CLK and CLK50 phase relationships are maintained and minimum pulse width specifications are met.

FAST-to-SLOW or SLOW-to-FAST mode changes will occur on the next rising or falling edge of PCLK. It is important to remember that the transition time for operating frequency changes, which are dependent upon PCLK, will vary with the HS-82C85RH oscillator or EFI frequency.

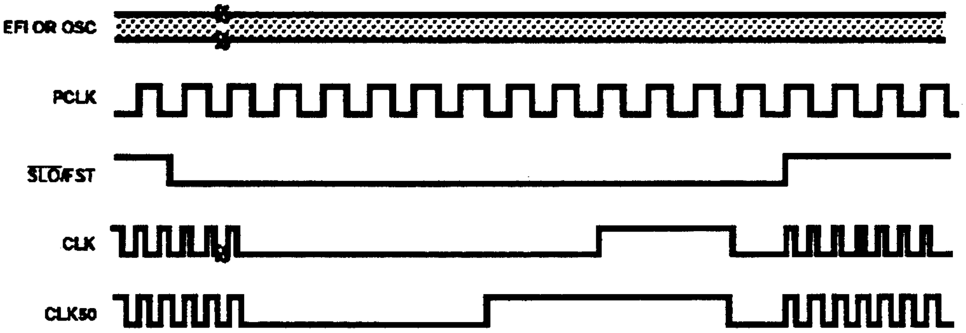


FIGURE 20. SLOW/FAST TIMING OVERVIEW

Slow/Fast Mode Control

The HS-82C55ARH programmable peripheral interface can be used to provide slow/fast mode control by connecting one of the port pins directly to the $\overline{\text{SLO}}$/FST pin (See Figure 21). With the port pin configured as an output, software control of the $\overline{\text{SLO}}$/FST pin is provided by simply writing a logical one (FAST mode) or logical zero (SLOW Mode) to the corresponding port. PORT C is well-suited for this function due to its bit set and reset capabilities.

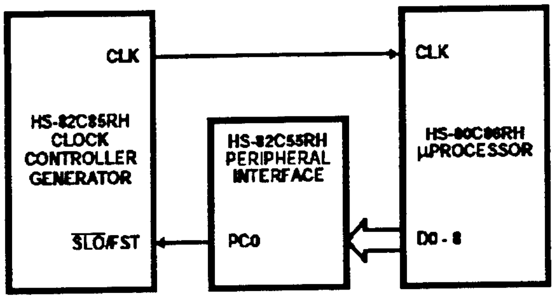


FIGURE 21. SLOW/FAST MODE CONTROL USING HS-82C55RH PERIPHERAL INTERFACE

Alternate Operating Modes

Using alternate modes of operation (slow, stop-clock, stop-oscillator) will reduce the average system operating power dissipation in a static CMOS system (See Table 2). This does not mean that system speed or throughput must be reduced. When used appropriately, the slow, stop-clock, stop-oscillator modes can make your design more power-efficient while maintaining maximum system performance.

TABLE 2. TYPICAL SYSTEM POWER SUPPLY CURRENT FOR STATIC CMOS OPERATING MODES

	FAST	SLOW	STOP-CLOCK	STOP-OSC
CPU Frequency	5MHz	20KHz	DC	DC
XTAL Frequency	15MHz	15MHz	15MHz	DC
IDD				
HS-80C86RH	50mA	2.5mA	250µA	250µA
HS-82C85RH	24.7mA	16.9mA	14.1mA	24.4µA
HS-82C08RH	1.0mA	10.0µA	1.0µA	1.0µA
82C82	1.7mA	6.5mA	1.0µA	1.0µA
HS-82C54RH	943.0µA	915.0µA	1.0µA	1.0µA
HS-82C55ARH	3.2µA	1.2µA	1.0µA	1.0µA
74HCXX + Other	2.9mA	110.0µA	90.0µA	90.0µA
HS-65262RH	4.0mA	50.0µA	10.0µA	10.0µA
HS-6617RH	6.3mA	52.5µA	12.0µA	12.0µA

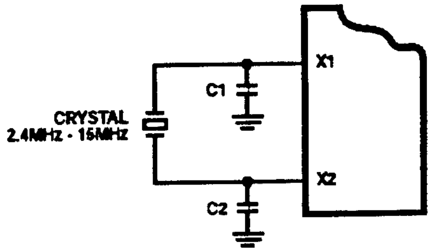
NOTE: All measurements taken at room temperature, VDD = +5.0V. Power supply current levels will be dependent upon system configuration and frequency of operation.

Oscillator

The oscillator circuit of the HS-82C85RH is designed primarily for use with an external parallel resonant, fundamental mode crystal from which the basic operating frequency is derived. The crystal frequency must be three times the required CPU clock. X1 and X2 are the two crystal input connections. The output of the oscillator is buffered and available at the OSC output (pin 18) for generation of other system timing signals.

For the most stable operation of the oscillator (OSC) output circuit, two capacitors (C1 = C2) are recommended. Capacitors C1 and C2 are chosen such that their combined capacitance matches the load capacitance as specified by the crystal manufacturer. This insures operation within the frequency tolerance specified by the crystal manufacturer.

The crystal/capacitor configuration and the formula used to determine the capacitor values are shown in Figure 22. Crystal Specifications are shown in Table 3. For additional information on crystal operation, see Harris publication Tech Brief 47.



$$CT = \frac{C1 \bullet C2}{C1 + C2}$$ (Including stray capacitance)

FIGURE 22. CRYSTAL CONNECTION

TABLE 3. CRYSTAL SPECIFICATIONS

PARAMETER	TYPICAL CRYSTAL SPECIFICATION
Frequency	2.4MHz to 15MHz
Type of Operation	Parallel Resonant, Fund. Mode
Load Capacitance	20pF or 32pF
R SERIES (Max)	56Ω (f = 15MHz, CL = 32pF), 105Ω (f = 15MHz, CL = 20pF)

Frequency Source Selection

The F/$\overline{\text{C}}$ input is a strapping pin that selects either the crystal oscillator or the EFI input as the source frequency for clock generation. If the EFI input is selected as the source, the oscillator section (OSC output) can be used independently for another clock source. If a crystal is not used, then crystal input X1 (pin 23) must be tied to VDD or GND and X2 (pin 22) should be left open. If the EFI mode is not used, then EFI (pin 20) should be tied to VDD or GND.

Clock Generator

The clock generator consists of two synchronous divide-by-three counters with special clear inputs that inhibit the counting. One counter generates a 33% duty cycle waveform (CLK) and the other generates a 50% duty cycle waveform (CLK50). These two counters are negative-edge synchronized, with the low-going transitions of both waveforms occurring on the same oscillator transition.The CLK and CLK50 output frequencies are one-third of the base input frequency when $\overline{\text{SLO}}$/FST is high and are equal to the base input frequency divided by 768 when $\overline{\text{SLO}}$/FST is low.

The CLK output is a 33% duty cycle clock signal designed to drive the HS-80C86RH microprocessor directly. CLK50 has a 50% duty cycle output synchronous with CLK, designed to drive coprocessors and peripherals requiring a 50% duty cycle clock.

PCLK is a peripheral clock signal with an output frequency equal to the oscillator or EFI frequency divided by 6. PCLK has a 50% duty cycle. PCLK is unaffected by $\overline{\text{SLO}}$/FST. When the HS-82C85RH is placed in the STOP mode, PCLK will remain in its current state (logic high or logic low) until a $\overline{\text{RES}}$ or START command restarts the HS-82C85RH clock circuitry. PCLK is negative-edge synchronized with CLK and CLK50.

Since PCLK continues to run at the same frequency regardless of the state of the $\overline{\text{SLO}}$/FST pin, it can be used by other devices in the system which need a fixed high frequency clock. For example, PCLK could be used to clock an HS-82C54RH programmable interval timer to produce a real-time clock for the system or as a baud rate generator to maintain serial data communications during SLOW mode operation.

Clock Synchronization

The clock synchronization (CSYNC) input allows the output clocks to be synchronized with an external event (such as another HS-82C85RH clock signal). CSYNC going active causes all clocks (CLK, CLK50 and PCLK) to stop in the HIGH state.

It is necessary to synchronize the CSYNC input to the EFI clock using two flip-flops as shown in Figure 23. Multiple external flip-flops are necessary to minimize the occurrence of metastable (or indeterminate) states.

Ready Synchronization

Two RDY inputs (RDY1, RDY2) are provided to accommodate two system buses. Each RDY input is qualified by its corresponding $\overline{\text{AEN}}$ input ($\overline{\text{AEN1}}$, $\overline{\text{AEN2}}$). Reception of a valid RDY signal causes the HS-82C85RH to output READY high, informing the HS-80C86RH that the pending data transfer may be concluded. (See HS-80C86RH data sheet system timing).

Synchronization is required for all asynchronous active-going edges of either RDY input to guarantee that the RDY set up and hold times are met. Inactive-going edges of RDY in normally ready systems do not require synchronization but must satisfy RDY setup and hold as a matter of proper system design.

The $\overline{\text{ASYNC}}$ input defines two modes of RDY synchronization operation. When $\overline{\text{ASYNC}}$ is LOW, two stages of synchronization are provided for active RDY input signals. Positive-going asynchronous RDY inputs will first be synchronized to flip-flop one at the rising edge of CLK (requiring a setup time TR1VCH) and then synchronized to flip-flop two at the next falling edge of CLK, after which time the READY output will go HIGH.

Negative-going asynchronous RDY inputs will be synchronized directly to flip-flop two at the falling edge of CLK, after which time the RDY output will go inactive. This mode of operation is intended for use by asynchronous (normally not ready) devices in the system which cannot be guaranteed by design to meet the required RDY setup timing (TR1VCL) on each bus cycle.

When $\overline{\text{ASYNC}}$ is high or left open, the first RDY flip-flop is bypassed in the RDY synchronization logic. RDY inputs are synchronized by flip-flop two on the falling edge of CLK before they are presented to the processor. This mode is available for synchronous devices that can be guaranteed to meet the required RDY setup time. $\overline{\text{ASYNC}}$ can be changed on every bus cycle to select the appropriate mode of synchronization for each device in the system.

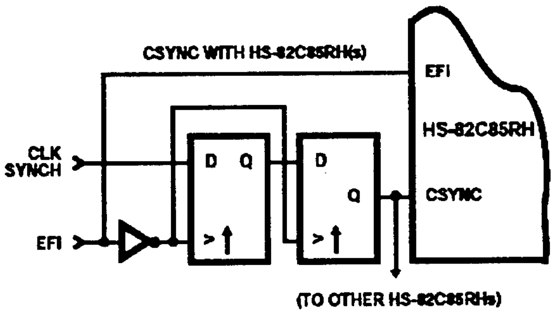


FIGURE 23. CSYNC SYNCHRONIZATION METHODS

Metallization Topology

DIE DIMENSIONS:

2770μm x 3130μm x 483μm ± 25μm

METALLIZATION:

Type: Al/Si

Thickness: 11kÅ ± 2kÅ

GLASSIVATION:

Type: SiO2

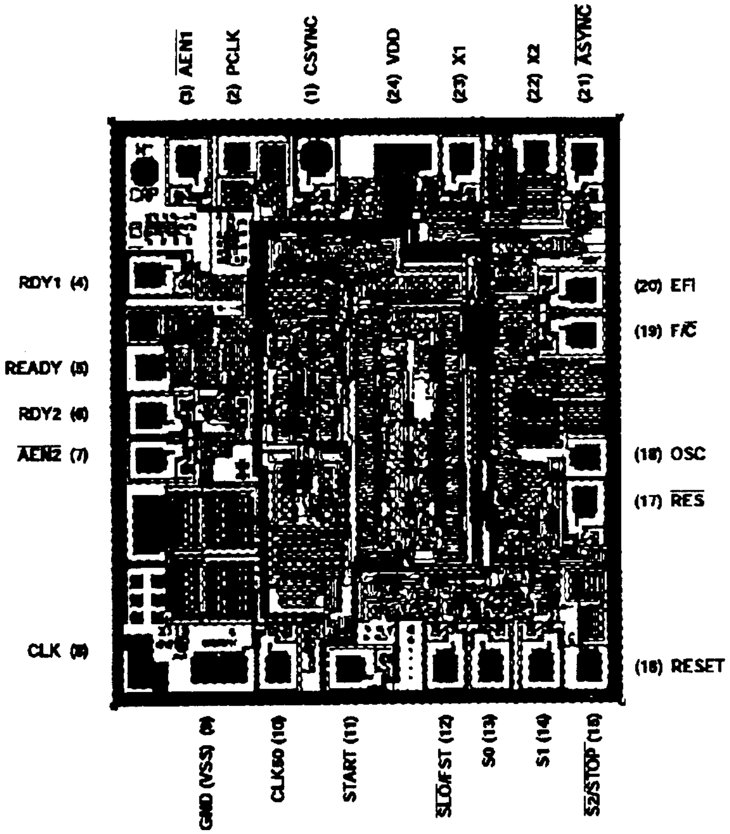
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:

1.6×10^4 A/cm^2

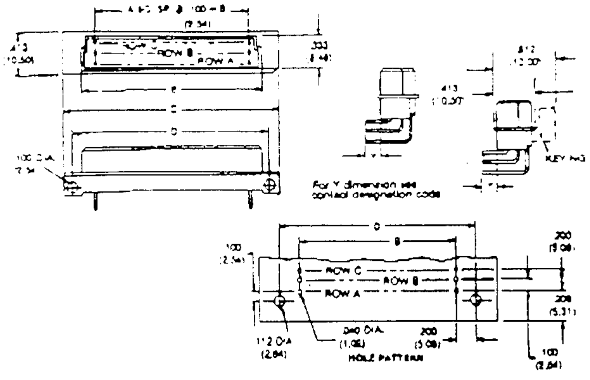
Metallization Mask Layout

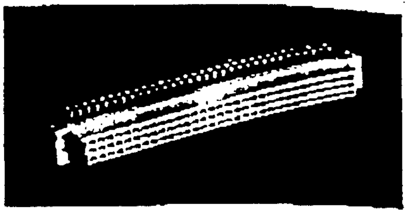
HS-82C85RH



Style R, 1/2 R & R-Expanded Receptacle 8477

Inverted 3-Row





ORDERING CODE Typical Example

20 **8477** **048** **002** **025**

PREFIX

20-SOCKET WITHOUT KEYING
22-SOCKET WITH KEYING
25-SOCKET WITH BOARD RETENTION CLIP FOR .062" (1.6mm) BOARD WITHOUT KEYING
27-SOCKET WITH BOARD RETENTION CLIP FOR .062" (1.6mm) BOARD WITH KEYING

SERIES

Inverted DIN, Style R & 1/2 R & expanded

NUMBER OF CONTACT CAVITY POSITIONS

NO. CONTACT POSITIONS	CONTACT ROWS	A	B	C	D	E
048	3 (3 X 16)	15	1.500 (38.10)	2.122 (53.90)	1.900 (48.26)	1.744 (44,30)
096	3 (3 X 32)	31	3.100 (78.74)	3.697 (93.90)	3.500 (88.90)	3.343 (84.91)
150	3 (3 X 50)	49	4.900 (124.46)	5.496 (139.60)	5.300 (134.62)	5.142 (130.61)

CONTACT DESIGNATION CODE

CODE NO.		DESCRIPTION	TERMINAL LENGTH = Y
002		Right angle P.C. contact sq. terminal	.118 (3.00)
006		Right-angle P.C. contact .012 (0.30) x .031 (0.79) terminal	.118 (3.00)
009		Right-angle P.C. contact .012 (0.30) x .031 (0.79) terminal	.177 (4.50)

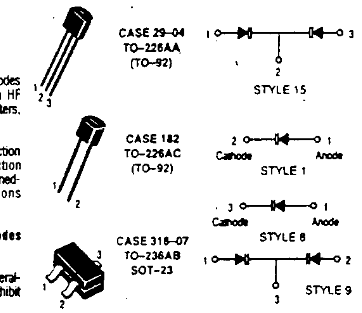
CODE NO.		DESCRIPTION	TERMINAL LENGTH=Y
012		Right-angle PC contact square terminal	.177 (4,50)
008		Right-angle wire wrap	.450 (11,4)

VARIATION CODE

	Gold All Over		Gold Contact Area, Tin/Lead Terminal		
Class	DIN 41612 Class II	DIN 41612 Class III	DIN 41612 Class II	DIN 41612 Class III	
Cycle Life	400 Cycles	50 Cycles	400 Cycles	50 Cycles	
	Variation Code Numbers				Contact Loading Positions
	097	073	025	001	Fully loaded .100 (2,54) grid
	098	074	026	002	Row A&C Fully loaded .100 (2.54) x .200 (5.08) grid

NOTE: For alternate loading and plating, please contact factory.
Shaded variations recommended for standard applications.
Available through ELCO franchised distributors.

Abrupt Junction Tuning Diodes



Motorola supplies voltage-variable capacitance diodes serving the entire range of frequencies from HF through UHF. Used in RF receivers and transmitters, they have a variety of applications.

Two families of devices are available: Abrupt Junction and Hyper Abrupt Junction. The Abrupt Junction family includes devices suitable for virtually all tuned-circuit and narrow-range tuning applications throughout the spectrum.

General Purpose Plastic abrupt Tuning Diodes
Capacitance Ratio @ 2.0 Volts/30 Volts
Case 182 — TO-226AC (TO-92) — 2-Lead
The following is a listing of plastic package, general-purpose, abrupt tuning diodes. These devices exhibit high Q characteristics.

Mfr.'s Type	C_T @ V_R=4.0 V, 1.0 MHz			$V_{(BR)R}$ (V)	Cap. Ratio C4/C30 Min.	Q 4.0 V, 50 MHz Typ.
	(pF) Min.	(pF) Nominal	(pF) Max.			
MV2101	6.1	6.8	7.5	30	2.5	400
MV2104	10.8	12.0	13.2	30	2.5	350
MV2108	24.3	27.0	29.7	30	2.5	250
MV2109	29.7	33.0	36.3	30	2.5	200
MV2111	42.3	47.0	51.7	30	2.5	150
MV2115	90.0	100.0	110.0	30	2.6	100

Abrupt Tuning Diodes for FM Radio — Dual
Case 29-04 — TO-226AA (TO-92)
The following is a listing of abrupt tuning diodes that are available as dual units in a single package.

Mfr.'s Type	C_T @ V_R[2]			Cap Ratio C3/C30 Min.	Q 3.0 V, 50 MHz Min.	$V_{(BR)R}$ (V)	Device Marking	Style
	(pF) Min.	(pF) Max.	(V)					
MV104	37	42	3.0	2.5	100	32	—	15

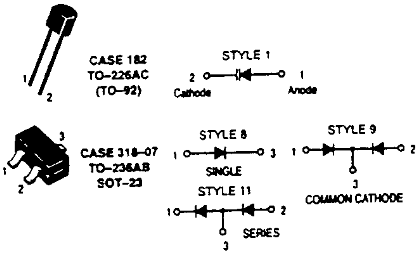
Abrupt Tuning Diodes for FM Radio — Dual
Case 318-07 — TO-236 AB (SOT-23)

MMBV432LT1	43	48.1	2.0	1.5[1]	100	14	M4B	9

[1] C2/C8. [2] Each Diode.

Hot-Carrier (Schottky) Diodes

Hot-Carrier diodes are ideal for VHF and UHF mixer and detector applications as well as many higher frequency applications. They provide stable electrical characteristics by eliminating the point-contact diode presently used in many applications



Hot-Carrier (Schottky) Diodes

Case 182 — TO-226AC (TO-92)
The following is a listing of hot carrier (Schottky) diodes that exhibit low forward voltage drop for improved circuit efficiency.

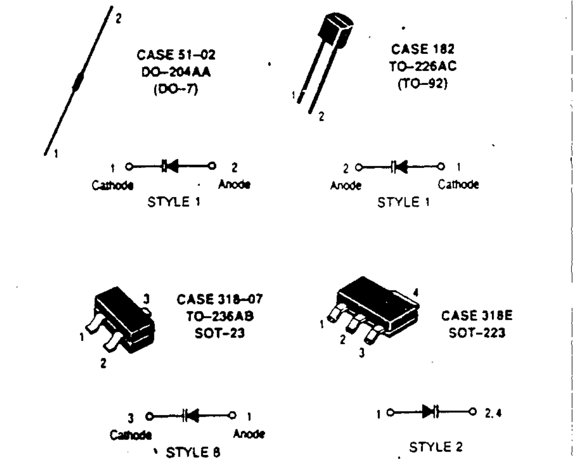
Mfr.'s Type	$V_{(BR)R}$ (V)	C_T @ V_R (pF) Max.	V_F @ 10 mA (V) Max.	I_R @ V_R (nA) Max.	Minority Lifetime (ps) Typ.	Device Marking	Style
MBD701	70.0	1.0 @ 20 V	1.0	200 @ 35.0 V	15	—	1
MBD301	30.0	1.5 @15 V	0.6	200 @ 25.0 V	15	—	1
MBD101	7.0	1.0 @ 0 V	0.6	250 @ 3.0 V	—	—	1

Case 318-07 — TO-236AB (SOT-23)

MMBD701LT1	70.0	1.0 @ 20 V	1.0	200 @ 35.0 V	15	5H	8
MMBD301LT1	30.0	1.5 @ 15 V	0.6	200 @ 25.0 V	15	4T	8
MMBD101LT1	7.0	1.0 @ 0 V	0.6	250 @ 3.0 V	—	4M	8
MMBD352LT1[1]	7.0	1.0 @ 0 V	0.6	250 @ 3.0 V	—	M5G	11
MMBD354LT1[1]	7.0	1.0 @ 0 V	0.6	250 @ 3.0 V	—	M6H	9

[1] Dual diodes.

Hyper Abrupt Junction Tuning Diodes



Tuning Diodes — Hyper-Abrupt Junction

The Hyper-Abrupt family exhibits higher capacitance, and a much larger capacitance ratio. It is particularly well sude wider-range application such as AM/FM radio and TV tuning.

Hyper-Abrupt Tuning Diodes For Telecommunications — Single
Case 182 — TO-226AC (TO-92)
The following is a listing of hyper-abrupt tuning diodes intended for high frequency, FM radio, and TV tuner applicatio

Mfr.'s Type	C_T @ V_R (f=1.0 MHz)			Cap. Ratio @ V_R			Q		$V_{(BR)R}$ (V)	Device Marking	Ca St
	(pF) Min.	(pF) Max.	(V)	Min.	Max.	(V)	3.0 V Min.	50 MHz Max.			
MV209	26.0	32.0	3.0	5.0	6.5	3/25	200	—	30	—	

Hyper-Abrupt Tuning Diodes For Telecommunications — Single
Case 318-07 — TO-236AB (SOT-23)

MMBV105GLT1	1.8	2.8	25.0	4.0	6.0	3/25	200	—	30	M4E	
MMBV109LT1	26.0	32.0	3.0	5.0	6.5	3/25	200	—	30	M4A	
MMBV409LT1	26.0	32.0	3.0	1.5	2.0	3/8	200	—	20	X5	
MMBV3102LT1	20.0	25.0	3.0	4.5	—	3/25	200	—	30	M4C	

Hyper-Abrupt Tuning Diodes For Communications — Dual
Case 318-07 — TO-236AB (SOT-23)

MMBV609LT1	26.0	32.0	3.0	1.8	2.4	3/8	250	—	20	5L	

Hyper-Abrupt Tuning Diodes For Low Frequency Applications — Single
Case 182 — TO-226AC (TO-92)
The following is a listing of AM, hyper-abrupt tuning diodes that have a large capacity range and redesigned fo frequency circuit applications.

Mfr.'s Type	C_T @ 1.0 MHz			Cap. Ratio @ V_R		$V_{(BR)R}$ (V)	Styl
	(pF) Min.	(pF) Max.	(V)	Min.	(V)		
MVAM108	440	560	1.0	15	1.0/8.0	12	1
MVAM109	400	520	1.0	12	1.0/9.0	15	1
MVAM115	440	560	1.0	15	1.0/15.0	18	1
MVAM125	440	560	1.0	15	1.0/25.0	28	1

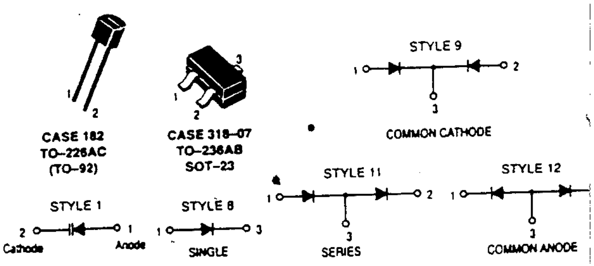
Hyper-Abrupt High Capacitance Voltage Variable Diode — Surface Mount
Pinout: 1 — Anode, 2, 4 — Cathode, 3 — NC, (Case 318E — SOT-223)
The following are high capacitance voltage variable diodes intended for low frequency applications and circuits req large tuning capacitance.

Mfr.'s Type	$V_{(BR)R}$ (V)	I_R nA	C_T @ f=1.0 MHz		Cap. Ratio Min.	Q Min.	Style
			(pF) Min.	(pF) Max.			
MV7005T1	15	100	400	520	12[1]	150[3]	2
MV7404T1	12	100	96	144	10[2]	200[4]	2

[1] V_R=1.0 V/V_R=9.0 V. [2] V_R=2.0 V/V_R=10 V. [3] V_R=1.0 V, f=1.0 MHz. [4] V_R=2.0 V, f=1.0 MHz.

Switching Diodes

Small-signal switching diodes are intended for low current switching and steering applications. Hot-Carrier, PIN and general-purpose diodes allow a wide selection for specific application requirements.



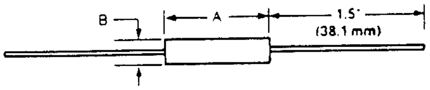
PIN Switching Diodes

Case 182 — TO-226AC (TO-92)
The following PIN diodes are designed for VHF band switching and general-purpose low current switching applications.

Mfr.'s Type	$V_{(BR)R}$ (V) Min.	C_T @ V_R @ 1.0 MHz		I_R @ V_R (nA) Max.	Series Resistance (Ω) Max.	Device Marking	Style
		(pF) Max.	(V)				
MPN3700	200	1.0	20	0.1 @ 150	1.00 @ 10 mA	—	1
MPN3404	20	2.0	15	0.1 @ 25 V	0.85 @ 10 mA	—	1

OHMITE

treous Enamel Molded ewound Resistors



Dimensions

Power Rating	Max. Length-A		Max. Dia.-B		Leads Ga.	Weight (g)
	In.	mm	In.	mm		
1½ W	.437	11.1	.140	3.6	24	.50
2¼ W	.390	9.9	.219	5.6	20	.80
3¼ W	.562	14.3	.234	5.9	20	1.20
5 W	.953	24.2	.234	5.9	20	1.80
11 W	1.796	45.6	.343	8.7	20	6.40

Features

- ▶ Molded Construction Provides Consistent Shape And Size (Permits Mounting In Clips Which Extends Power Rating)
- ▶ Meets Mil-R-26 Requirements For Insulated Resistors
- ▶ All-Welded Construction
- ▶ Flame Resistant Vitreous Enamel Coating
- ▶ 5% Tolerance

Molded construction provides consistent shape and size which permits mounting in clips to extend power rating. Mechanical integrity is enhanced by the all-welded construction and the vitreous enamel coating is flame resistant. The durable vitreous enamel coating, which is silicone-free, permits the resistors to maintain a hard coating while operating at high temperatures. Ceramic core with solder coated axial leads.

1½ Watts

Stock No.	Mfr.'s Type	Ohms	EACH	
			1-49	50-99
96-0655	91J1R0	1	3.55	3.02
296-0656	91J1R5	1.5	3.55	3.02
296-0657	91J2R0	2	3.55	3.02
296-0660	91J2R4	2.4	3.55	3.02
296-0658	91J2R7	2.7	3.55	3.02
296-0659	91J3R3	3.3	3.55	3.02
296-0661	91J10R	10	2.80	2.38
296-0662	91J15R	15	2.80	2.38
296-0663	91J18R	18	2.80	2.38
296-0664	91J22R	22	2.80	2.38
296-0666	91J33R	33	2.80	2.38
296-0667	91J36R	36	2.80	2.38
296-0668	91J47R	47	2.80	2.38
296-0669	91J50R	50	2.80	2.38
296-0671	91J75R	75	2.80	2.38
296-0672	91J91R	91	2.80	2.38
296-0665	91J100	100	3.08	2.62
296-0673	91J120	120	3.08	2.62
296-0674	91J180	180	3.08	2.62
296-0676	91J220	220	3.08	2.62
296-0677	91J270	270	3.08	2.62
296-0678	91J330	330	3.08	2.62
296-0679	91J470	470	3.08	2.62
296-0681	91J620	620	3.08	2.62
296-0682	91J820	820	3.08	2.62
296-0670	91J1K0	1K	3.15	2.68
296-0683	91J1K2	1.2K	3.15	2.68
296-0684	91J1K5	1.5K	3.15	2.68
296-0686	91J2K0	2K	3.15	2.68
296-0687	91J2K2	2.2K	3.15	2.68

2¼ Watts

296-0688	92J1R0	1	1.73	1.47
296-0689	92J1R5	1.5	1.73	1.47
296-0691	92J2R0	2	1.73	1.47
296-0692	92J2R2	2.2	1.73	1.47
296-0693	92J3R0	3	1.73	1.47
296-0694	92J3R3	3.3	1.73	1.47
296-0696	92J4R0	4	1.73	1.47
296-0697	92J4R7	4.7	1.73	1.47
296-0698	92J7R5	7.5	1.73	1.47
296-0699	92J10R	10	1.45	1.23

2¼ Watts (continued)

Stock No.	Mfr.'s Type	Ohms	EACH	
			1-49	50-99
296-0701	92J15R	15	1.45	1.23
296-0702	92J22R	22	1.45	1.23
296-0703	92J47R	47	1.45	1.23
296-0704	92J62R	62	1.45	1.23
296-0706	92J100	100	1.45	1.23
296-0707	92J120	120	1.45	1.23
296-0708	92J180	180	1.45	1.23
296-0709	92J220	220	1.45	1.23
296-0711	92J270	270	1.45	1.23
296-0712	92J330	330	1.45	1.23
296-0713	92J390	390	1.45	1.23
296-0675	92J470	470	1.45	1.23
296-0714	92J510	510	1.84	1.56
296-0716	92J680	680	1.84	1.56
296-0717	92J820	820	1.84	1.56
296-0718	92J1K0	1K	2.11	1.79
296-0680	92J1K2	1.2K	2.11	1.79
296-0685	92J1K8	1.8K	2.11	1.79

3¼ Watts

296-0690	93J1R0	1	1.44	1.22
296-0695	93J2R0	2	1.44	1.22
296-0722	93J3R0	3	1.44	1.22
296-0700	93J4R7	4.7	1.44	1.22
296-0723	93J5R0	5	1.44	1.22
296-0724	93J10R	10	1.21	1.03
296-0726	93J15R	15	1.21	1.03
296-0727	93J16R	16	1.21	1.03
296-0728	93J22R	22	1.21	1.03
296-0729	93J33R	33	1.21	1.03
296-0731	93J39R	39	1.21	1.03
296-0732	93J47R	47	1.21	1.03
296-0705	93J50R	50	1.21	1.03
296-0733	93J68R	68	1.21	1.03
296-0734	93J82R	82	1.21	1.03
296-0710	93J100	100	1.21	1.03
296-0736	93J120	120	1.21	1.03
296-0737	93J130	130	1.21	1.03
296-0738	93J150	150	1.21	1.03
296-0739	93J180	180	1.21	1.03
296-0715	93J220	220	1.21	1.03
296-0741	93J270	270	1.21	1.03
296-0742	93J330	330	1.21	1.03
296-0743	93J390	390	1.21	1.03
296-0744	93J470	470	1.21	1.03
296-0746	93J510	510	1.55	1.32
296-0747	93J680	680	1.55	1.32
296-0748	93J820	820	1.55	1.32
296-0720	93J1K0	1K	1.76	1.50
296-0749	93J1K8	1.8K	1.76	1.50
296-0751	93J2K0	2K	1.76	1.50
296-0725	93J2K4	2.4K	1.76	1.50
296-0752	93J3K3	3.3K	2.15	1.83
296-0753	93J4K0	4K	2.15	1.83
296-0754	93J4K7	4.7K	2.15	1.83
296-0756	93J5K0	5K	2.48	2.11
296-0730	93J5K6	5.6K	2.48	2.11
296-0735	93J6K8	6.8K	2.48	2.11
296-0740	93J10K	10K	2.48	2.11

5 Watts

296-0745	95J1R0	1	1.72	1.46
296-0757	95J1R2	1.2	1.72	1.46
296-0758	95J2R0	2	1.72	1.46
296-0759	95J2R4	2.4	1.72	1.46
296-0761	95J3R0	3	1.72	1.46
296-0762	95J3R3	3.3	1.72	1.46
296-0763	95J4R0	4	1.72	1.46
296-0750	95J5R0	5	1.72	1.46
296-0755	95J6R8	6.8	1.72	1.46
296-0760	95J10R	10	1.52	1.29
296-0764	95J15R	15	1.52	1.29
296-0766	95J18R	18	1.52	1.29
296-0767	95J22R	22	1.52	1.29
296-0768	95J25R	25	1.52	1.29
296-0769	95J30R	30	1.52	1.29

5 Watts (continued)

Stock No.	Mfr.'s Type	Ohms	EACH	
			1-49	50-99
296-0765	95J33R	33	1.52	1.29
296-0771	95J39R	39	1.52	1.29
296-0772	95J40R	40	1.52	1.29
296-0770	95J50R	50	1.52	1.29
296-0773	95J62R	62	1.52	1.29
296-0774	95J75R	75	1.52	1.29
296-0776	95J82R	82	1.52	1.29
296-0775	95J100	100	1.52	1.29
296-0777	95J120	120	1.52	1.29
296-0778	95J150	150	1.52	1.29
296-0779	95J180	180	1.52	1.29
296-0781	95J200	200	1.52	1.29
296-0782	95J220	220	1.52	1.29
296-0783	95J250	250	1.52	1.29
296-0784	95J270	270	1.52	1.29
296-0786	95J330	330	1.52	1.29
296-0787	95J400	400	1.52	1.29
296-0788	95J470	470	1.52	1.29
296-0780	95J1K0	1K	1.84	1.56
296-0789	95J1K2	1.2K	2.14	1.82
296-0791	95J1K5	1.5K	2.14	1.82
296-0792	95J2K0	2K	2.14	1.82
296-0785	95J2K5	2.5K	2.50	2.13
296-0793	95J3K0	3K	2.50	2.13
296-0794	95J3K3	3.3K	2.50	2.13
296-0796	95J4K7	4.7K	2.50	2.13
296-0790	95J5K0	5K	3.04	2.58
296-0795	95J5K6	5.6K	3.04	2.58
296-0797	95J6K0	6K	3.04	2.58
296-0800	95J10K	10K	3.04	2.58
296-0805	95J12K	12K	3.04	2.58
296-0801	95J15K	15K	3.04	2.58
296-0810	95J16K	16K	3.04	2.58
296-0803	95J18K	18K	3.04	2.58
296-0815	95J20K	20K	3.63	3.09
296-0806	95J25K	25K	3.63	3.09

11 Watts

296-0605	90J5R0	5	2.31	1.96
296-0597	90J10R	10	2.31	1.96
296-0598	90J11R	11	2.31	1.96
296-0599	90J15R	15	2.31	1.96
296-0609	90J20R	20	2.31	1.96
296-0611	90J22R	22	2.31	1.96
296-0612	90J25R	25	2.31	1.96
296-0613	90J30R	30	2.31	1.96
296-0610	90J33R	33	2.31	1.96
296-0614	90J47R	47	2.31	1.96
296-0616	90J50R	50	2.31	1.96
296-0615	90J62R	62	2.31	1.96
296-0617	90J75R	75	2.31	1.96
296-0618	90J82R	82	2.31	1.96
296-0620	90J100	100	2.28	1.94
296-0621	90J120	120	2.28	1.94
296-0622	90J150	150	2.28	1.94
296-0633	90J220	220	2.28	1.94
296-0634	90J270	270	2.28	1.94
296-0625	90J330	330	2.28	1.94
296-0636	90J600	600	2.61	2.22
296-0637	90J1K0	1K	2.92	2.48
296-0638	90J1K2	1.2K	2.92	2.48
296-0639	90J1K3	1.3K	2.92	2.48
296-0641	90J1K5	1.5K	2.92	2.48
296-0642	90J2K0	2K	2.92	2.48
296-0630	90J2K5	2.5K	3.29	2.80
296-0631	90J5K0	5K	3.85	3.27
296-0632	90J7K5	7.5K	3.85	3.27
296-0635	90J10K	10K	3.85	3.27
296-0644	90J12K	12K	3.85	3.27
296-0640	90J15K	15K	3.85	3.27
296-0646	90J18K	18K	3.85	3.27
296-0649	90J20K	20K	4.46	3.79
296-0643	90J25K	25K	4.46	3.79
296-0645	90J27K	27K	4.46	3.79
296-0647	90J30K	30K	4.46	3.79
296-0648	90J33K	33K	4.46	3.79
296-0650	90J50K	50K	4.46	3.79

Microprocessor Crystal Units

Specifications

Nominal Frequency	Type B HC-33/U 1.000 MHz - 4.000 MHz Type A HC-49/U 1.800 MHz - 300.000 MHz Type C HC-45/U 3.579545 MHz - 300,000 MHz
Frequency Tolerance at 25° C	± 30 ppm typ (± 50 ppm max)
Frequency Stability over Temperature -20° C to + 70° C	± 50 ppm typ (± 100 ppm max)
Aging	± 5 ppm / year
Load Capacitance	12 to 32 pF
Shunt Capacitance	7 pF max
Drive Level	1mW

Part Numbering System

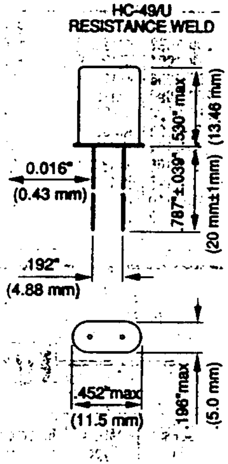
Example: A-3.579545-18

Example: A-32.000-18-FUND

A	3.579545	18	Optional
Holder Type A - HC-49/U B - HC-33/U C - HC-45/U C-SMD - HC-45/U SMD	Frequency (in MHz)	• Load Capacitance, (12pF - 32pF) For Parallel Resonance • S - For Series Resonance	3RD - Third Pin SL - Plastic Sleeve SB - Plastic Spacer FUND - Fundamental (For over 20 MHz Only) 30T - 3rd Overtone 50T - 5th Overtone 70T - 7th Overtone 90T - 9th Overtone

Stock No.	Mfr.'s Type	Freq. (MHz)	Holder	Ω*	EACH	
					1-99	100-Up
996-0100	A-1.000-18	1.000000	HC49/U	—	8.07	7.26
996-0110	A-1.8432-18	1.843200	HC49/U	700	2.51	2.26
996-0120	A-2.4576-18	2.457600	HC49/U	400	2.21	1.99
996-0130	A-3.579545-18	3.579545	HC49/U	180	1.17	1.05
996-0140	A-3.6864-18	3.686400	HC49/U	160	1.20	1.08
996-0150	A-4.000-18	4.000000	HC49/U	100	1.20	1.08
996-0160	A-4.096-18	4.096000	HC49/U	100	1.20	1.08
996-0170	A-4.194304-18	4.194304	HC49/U	100	1.20	1.08
996-0180	A-6.000-18	6.000000	HC49/U	50	1.20	1.08
996-0190	A-6.144-18	6.144000	HC49/U	50	1.20	1.08
996-0200	A-7.3728-18	7.372800	HC49/U	40	1.20	1.08
996-0210	A-8.000-18	8.000000	HC49/U	35	1.20	1.08
996-0220	A-9.8304-18	9.830400	HC49/U	35	1.20	1.08
996-0230	A-11.0592-18	11.05920	HC49/U	30	1.20	1.08
996-0240	A-12.0000-18	12.00000	HC49/U	30	1.20	1.08
996-0250	A-12.288-18	12.28800	HC49/U	30	1.30	1.17
996-0260	A-14.31818-18	14.31818	HC49/U	25	1.30	1.17
996-0270	A-14.7456-18	14.74560	HC49/U	25	1.30	1.17
996-0280	A-15.000-18	15.00000	HC49/U	25	1.30	1.17
996-0290	A-16.000-18	16.00000	HC49/U	25	1.30	1.17
996-0300	A-18.432-18	18.43200	HC49/U	20	1.30	1.17
996-0310	A-20.000-18	20.00000	HC49/U	20	1.30	1.17
996-0320	A-24.000-18	24.00000	HC49/U	20	1.30	1.17
996-0330	A-24.5760-18	24.57600	HC49/U	40	1.30	1.17

* Maximum Equivalent Series Resistance (Ω)



Clock Oscillators - TTL Compatible

Specifications

Model		CO1000 Family - CO13000 Family	CO6000 Family
Package		14 Pin DIP 8 Pin DIP	14 Pin DIP
Frequency Range		250 KHz to 80 MHz	500 KHz to 70
Frequency Stability*		CO1100 / CO13100 - ± 100 ppm CO1050 / CO13050 - ± 50 ppm CO1025 / CO13025 - ± 25 ppm	CO6100 / CO12100 CO6050 / CO12050 CO6025 / CO12025
Temperature Range		Operating: 0° to +70° C	Storage: -55° C to
Input	Voltage	5V DC ± 0.5V DC	5V DC ± 0.5V D
	Current (MAX)	60mA - 250KHz to 2.999 MHz 35mA - 3 MHz to 31.999 MHz 45mA - 32 MHz to 80 MHz	20mA - 500KHz to 19. 30mA - 20.000 MHz to 40mA - 35.000 MHz to
Output	Symmetry	40 to 60% Normal, 45 to 55% Tight @ 1.4V DC	40 to 60% Norm 45 to 55% Tight @
	Rise and Fall Time	± 15ns max - Under 9 MHz ± 10ns max - 9 MHZ to 32 MHz ± 6ns max - 32 MHz to 80 MHz	10ns - 500KHz to 23. 6ns - 24.000 MHz to 70
	Logic "0"	0.4V max, Sink to 16mA	+0.5V (10% V
	Logic "1"	+2.4V min, Source 0.4mA	+4.5V (90% V
Output Load		1 to 10 TTL Loads	CL - 15pF (typ) (10 TT

*Frequency Stability inclusive of room tolerance, temperature stability over 0° C to +70° C, ± 10% power supply variation, aging, shock and vibration.

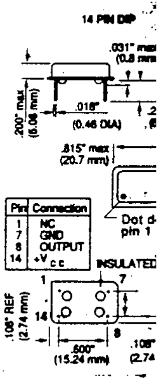
Part Numbering System

Example: CO1100-4.000-T

Example: (

CO1	100	4.000	O
Family CO1 - TTL, Full Size CO13 - TTL, Half Size CO6 - H CMOS, Full Size CO12 - H CMOS, Half Size	Frequency Stability 100 - 100 ppm 050 - 50 ppm 025 - 25 ppm	Frequency (in MHz)	Symmetry N - Normal (Usually O T - Tight (4

Stock No.	Mfr.'s Type	Freq. (MHz)	Holder (DIP)	EACH	
				1-99	100-Up
996-1100	CO1100-1.8432	1.843200	14 Pin	3.93	3.29
996-1110	CO1100-3.579545	3.579545	14 Pin	3.34	2.80
996-1120	CO1100-4.000	4.000000	14 Pin	3.34	2.80
996-1130	CO1100-10.000	10.00000	14 Pin	3.34	2.80
996-1140	CO1100-11.0592	11.05920	14 Pin	3.34	2.80
996-1150	CO1100-14.31818	14.31818	14 Pin	3.34	2.80
996-1160	CO1100-18.432	18.43200	14 Pin	3.34	2.80
996-1170	CO1100-24.000	24.00000	14 Pin	3.34	2.80
996-1180	CO1100-32.000	32.00000	14 Pin	3.34	2.80
996-1190	CO1100-36.000	36.00000	14 Pin	3.77	3.39
996-1200	CO1100-40.000	40.00000	14 Pin	3.77	3.39
996-1210	CO1100-48.000	48.00000	14 Pin	3.77	3.39
996-1220	CO1100-50.000	50.00000	14 Pin	3.77	3.39
996-1230	CO1100-66.666	66.66600	14 Pin	3.82	3.46
996-1240	CO1100-80.000	80.00000	14 Pin	6.56	5.63



ENVIRONMENTAL*

Temperature Cycle: ± 5 ppm max., 0 to 120° C, 3 cycles, 2 hours max. each, 25 ±2° C Ref.
Shock: 1000G's 0.35m sec, half sine wave, 3 shocks each plane.
Vibration: 10÷55Hz, 1.50mm D.A., 55-2000Hz, 35G's. Duration - 12 hours.
Humidity: 85% relative humidity, at +85° C, 250 hours.

MECHANICAL

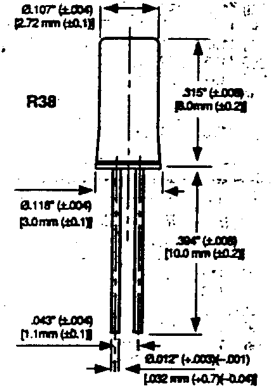
Gross Leak Test: All units 100% leak tested
Hermetically Sealed Package: Mass spectrometer leak 10^{-8} atoms. cc/sec. of heli
Seal Strength: 9kgs max. force perp. to t
Bend Test: Will withstand max. bend
Marking Ink: Epoxy, heat cured.
Solvent Resistance: Isopropyl alcohol, Trichlo

Tuning Fork Quartz Crystal Units 32.768 KHz

Specifications

Holder Type / Item	R38
Nominal Frequency 24° C	32.768 KHz ± 20 ppm
Turnover Temperature	24° C ± 4° C
Parabolic Curvature Constant	-0.035 ppm / °C typ
Quality Factor	80,000 typ / 50,000 min
Equivalent Series Resistance R_1	18K Ω typ
Motional Capacitance C_1	0.0035 pF typ
Shunt Capacitance C_0	1.7 pF typ
Capacitance Ratio	490 typ
Motional Inductance L_1	7 mH typ
Aging (First Year)	± 3 ppm
Operating Temperature Range	-10° C to +60° C
Storage Temperature Range	-30° C to +100° C

Stock No.	Mfr.'s Type	Each	
		1-24	25-49
996-2000	R38-32.768	0.50	0.35



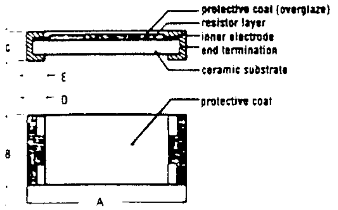
Also Available:

- ► Microprocessor Crystal Units HC-49 Short (AT Strip)
- ► Microprocessor Crystal Units Surface Mount - TT-SMD
- ► Clock Oscillators - Dual Output
- ► Clock Oscillators - Enable/Disable
- ► Clock Oscillators - ECL Compatible
- ► Clock Oscillators - HCMOS Compatible
- ► Voltage Controlled Crystal Oscillators - VCXO
- ► Temperature Compensated Crystal Oscillators - TCXO
- ► Monolithic Crystal Filters
- ► Ceramic Resonators - 200 to 800 KHz, 2.000 to 12.000 MHz

Raltron manufactures one of the most complete product lines of frequency m components including high quality crystal units, oscillators, filters, and c onators both through-hole and surface mount.

Because the product line is so complete, the inventory so large, Raltron an offer pricing that is always competitive, and often far lower than the competit

eri6 ; Commercial SMD Chip Resistors

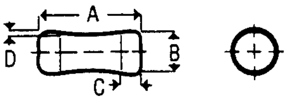


'e surface mounted chip resistor consists of a glass passivated thick film resistive paste screened onto a high purity alumina ramic substrate. The nominal resistance value is achieved by varying the composition of the paste prior to the screening process 'd by laser trimming the film after it has been screened on. To insure mechanical and environmental integrity, the chip is covered th a silicon based "procoat." The conductive layer consists of a precious metal and a wrap around termination is deposited at ch end to allow mechanical and electrical attachment. These chip resistors and adaptable to high speed automated mechanization sembly. They allow excellent printed circuit board density as well as utilization of both board sides. Zero ohm jumper available as stom order in full reels only.

Stock No.	Mfr.'s Type	Philips No.	Tol. %	Wattage @70°C	Value Range	Value Chart	Dimensions (In.)					PER PK./100	
							A	B	C	D	E	1-5	6-25
297-91XX	9C1206	9C12063A-FK	1	1/8	10 Ω to 1 M	D	.126	.063	.023	.016	.020	**3.73**	**3.00**
297-93XX	9C1206	9C12063A-JL	5	1/4	10 Ω to 1 M	C	.126	.063	.023	.016	.020	**2.76**	**2.29**
297-95XX	9C0805	9C08052A-JL	5	1/10	10 Ω to 1 M	C	.079	.049	.024	.016	.016	**3.31**	**2.63**
297-96XX	9C0805	9C08052A-FK	1	1/10	10 Ω to 1 M	D	.079	.049	.024	.016	.016	**4.08**	**3.26**

hart C 5% Values

Ohms	XX	Ohms	XX	Ohms	XX	Ohms	XX	Ohms	XX	Ohms	XX	Ohms	XX	Ohms	XX	Ohms	XX
10	10	39	18	200	26	470	34	2700	42	5600	50	30 K	58	100 K	66	390 K	74
20	12	47	20	270	28	560	36	3000	44	10 K	52	39 K	60	200 K	68	470 K	76
27	14	56	22	300	30	1000	38	3900	46	20 K	54	47 K	62	270 K	70	560 K	78
30	16	100	24	390	32	2000	40	4700	48	27 K	56	56 K	64	300 K	72	1 Meg	80



Series 9B Precision MELF Surface Mount Resistors

The MELF resistor consists of a high alumina core on which metal film is deposited. A cap is applied at each end and the resistor is spiralled to value. The resistor is then coated, color coded, and end caps treated to facilitate soldering. Zero ohm jumper available as custom order in full reels only.

Stock No.	Mfr.'s Type	Philips No.	Tol. %	Wattage @70°C	Value Range	Value Chart	Dimensions (In.)				PER PK./1000	
							A	B	C	D	1-9	10-49
2[illegible]X	9B0805	9B08052A-FC	1	1/8	10 Ω to 1 M	D	.087	.039	.014	.002	**130.00**	**120.00**
297-[illegible]XX	9B1406	9B14064A-FC	1	1/8	10 Ω to 1 M	D	.136	.055	.023	.006	**65.00**	**55.00**

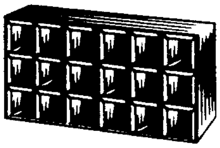
;hart D 1% Values

Ohms	XX	Ohms	XX	Ohms	XX	Ohms	XX	Ohms	XX	Ohms	XX	Ohms	XX	Ohms	XX
10	03	49.9	15	200	27	1 K	39	4.99 K	51	20 K	63	100 K	75	499 K	87
15	06	75	18	301	30	1.5 K	42	7.5 K	54	30.1 K	66	150 K	78	750 K	90
20	09	100	21	499	33	2 K	45	10 K	57	49.9 K	69	200 K	81	1 Meg	93
30.1	12	150	24	750	36	3.01 K	48	15 K	60	75 K	72	301 K	84	—	—

RCD Chip Resistor Kits

- Economical Pricing
- Great for Engineering Labs Or Prototyping
- Packaged In Plastic Boxes

Thick Film Kits



Thin Film Kits

0805 Thick Film 5%
Provides MC0805 5% parts, 122 values, 10 pieces each. 10 Ω to 1 M (including zero ohm) in 200 ppm parts. 1220 pieces total.
849-5000. 0805J10 .... **EACH 55.89**

0805 Thick Film 5%
Same as above, except 50 pieces each, 6100 pieces total.
849-5005. 0805J50 .... **EACH 116.65**

0805 Thick Film 1%
Provi[illegible] MCR0805 1% parts, 72 values, 10 pieces each. 10 Ω to [illegible]0 ppm parts. 720 pieces total.
849[illegible]0805F10 .... **EACH 58.50**

0805 Thick Film 1%
Same as above, except 50 pieces each, 3600 pieces total.
849-5015. 0805F50 .... **EACH 137.07**

1206 Thick Film 5%
Provides MC1A 5% parts, 24 values, 10 pieces each. 10 Ω to 1 M (including zero ohm) in 200 ppm parts. 240 pieces total.
849-5020. 1206C10 .... **EACH 25.00**

1206 Thick Film 5%
Provides MC1A 5% parts, 122 values, 10 pieces each. 10 Ω to 1 M (including zero ohm) in 200 ppm parts.1220 pieces total.
849-5025. 1206J10 .... **EACH 55.89**

1206 Thick Film 5%
Same as above, except 50 pieces each, 6100 pieces total.
849-5030. 1206J50 .... **EACH 115.00**

0805 Thin Film 0.5%
Provides BLU-0805 0.5% parts, 97 values, 100 pieces each. 10 Ω to 100 KΩ in 50 ppm parts. 9700 pieces total.
849-5035. B0805D100 .... **EACH 915.00**

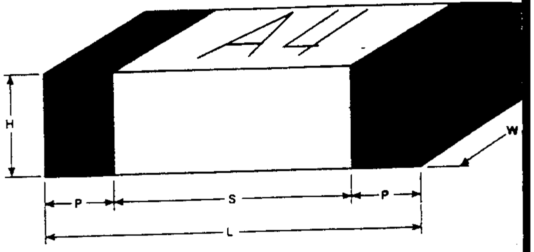
1206 Thin Film 1%
Provides BLU-1206 1% parts, 106 values, 100 pieces each. 10 Ω to 240 KΩ in 25 ppm parts. 10,600 pieces total.
849-5050. B1206F100 .... **EACH 1725.00**

SEI Kits

Surface mount thick film chip resistor design kits for RMC-1/8 (1206 size) in 5% and 1% tolerances, RMC-1/10 (0805 size) in 5% and 1% tolerances and RMC-1/16 (0603 size) in 5% tolerance only. Kits have 30 samples per value. 5% kits have 60 values (E24) and 1% kits have 120 values (E96). Kit includes product specifications, packaging guidelines, performance data and the chip samples. Replacement parts available in 1000 piece bulk packaging or 5000 piece tape and reel. Packaged in plastic notebook pages in three-ring binder.

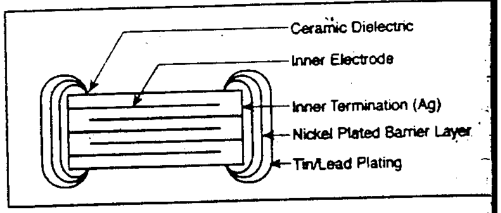
894-0100. RMC-1/8. 5% 1206 kit .... **EACH 79.00**
894-0105. RMC-1/8. 1% 1206 kit .... **EACH 115.50**
894-0110. RMC-1/10. 5% 0805 kit .... **EACH 79.00**
894-0115. RMC-1/10. 1% 0805 kit .... **EACH 115.50**
894-0120. RMC-1/16. 5% 0603 kit .... **EACH 107.75**

Monolithic SMD® Chip Capacitors



► Monolithic Construction

Monolithic ceramic capacitors consist of alternating ceramic (15 to 30 microns) onto which metal electrodes are printed. The stacked layers, cut into individual chips, are then sintered at a very high temperature to form a monolithic device. Alternating electrode layers are connected to end terminations completing the functional unit. **Temperature Characteristics:** C0G — 0 ±30 ppm/°C, –55°C to +125°C; X7R — ±15% ΔC, –55°C to +125°C; Y5V — +22% to –82% ΔC, –30°C to +85°C; Z5U — +22% to –56% ΔC, +10°C to +85°C. **Termination:** B — Ni/Sn. **Packaging:** B — T&R 7" reel; 2 — 7" paper tape. **Marking:** 0 — no mark.



CMC Case Size Dimensions — Millimeters (Inches)

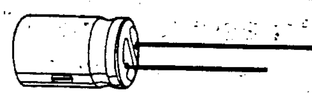
Case Size	Length (L)	Width (W)	Height (H)		Term. Width (P)		Spacing (S) Min.
			Min.	Max.	Min.	Max.	
0603	1.6 ± .10 (.063 ± .004)	0.80 ± .10 (.032 ± .004)	0.70 (.028)	0.90 (.036)	0.25 (.010)	0.65 (.026)	0.40 (.016)
0805	2.0 ± .10 (.079 ± .004)	1.25 ± .10 (.049 ± .004)	0.51 (.021)	1.30 (.052)	0.25 (.010)	0.75 (.030)	0.55 (.022)
1206	3.2 ± .15 (.126 ± .006)	1.6 ± .15 (.063 ± .006)	0.51 (.021)	1.60 (.064)	0.25 (.010)	0.75 (.030)	1.40 (.056)

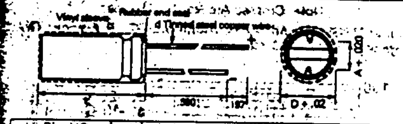
Stock No.	Mfr.'s Type	Value (pF)	Voltage	Temperature Coefficient	Tolerance	Reel Quantity	PER REEL
							1-9
748-5002	0603CG100J9B20	10	50 V	C0G	5%	4000	197.20
748-5004	0603CG180J9BB0	18	50 V	C0G	5%	4000	215.13
748-5008	0603CG220J9BB0	22	50 V	C0G	5%	4000	215.13
748-5010	0603CG270J9BB0	27	50 V	C0G	5%	4000	215.13
748-5012	0603CG470J9BB0	47	50 V	C0G	5%	4000	215.13
748-5016	0603CG101J9B20	100	50 V	C0G	5%	4000	215.13
748-5018	06032R331K9B20	330	50 V	X7R	10%	4000	178.04
748-5020	06032R102K9BB0	1000	50 V	X7R	10%	4000	178.04
748-5022	06032R222K9B20	2200	50 V	X7R	10%	4000	178.04
748-5024	06032R472K9BB0	4700	50 V	X7R	10%	4000	207.71
748-5026	06032R103K9BB0	10000	50 V	X7R	10%	4000	222.55
748-5028	06032F103M9B20	10000	50 V	Y5V	20%	4000	207.71
748-5030	06032F473M9B20	47000	50 V	Y5V	20%	4000	215.13
748-5032	06032F104M8B20	100000	25 V	Y5V	20%	4000	215.13
748-5034	0805CG100J9BB0	10	50 V	C0G	5%	4000	126.11
748-5036	0805CG150J9BB0	15	50 V	C0G	5%	4000	148.36
748-5040	0805CG220J9BB0	22	50 V	C0G	5%	4000	126.11
748-5042	0805CG270J9BB0	27	50 V	C0G	5%	4000	148.36
748-5044	0805CG330J9BB0	33	50 V	C0G	5%	4000	126.11
748-5046	0805CG470J9BB0	47	50 V	C0G	5%	4000	148.36
748-5050	0805CG560J9BB0	56	50 V	C0G	5%	4000	148.36
748-5052	0805CG680J9BB0	68	50 V	C0G	5%	4000	200.29
748-5054	0805CG101J9BB0	100	50 V	C0G	5%	4000	148.36
748-5056	0805CG221J9BB0	220	50 V	C0G	5%	4000	148.36
748-5058	0805CG271J9BB0	270	50 V	C0G	5%	4000	200.29
748-5060	0805CG331J9BB0	330	50 V	C0G	5%	4000	200.29
748-5062	0805CG471J9BB0	470	50 V	C0G	5%	3000	150.22
748-5064	0805CG102J9BB0	1000	50 V	C0G	5%	3000	122.40
748-5066	08052R102K9BB0	1000	50 V	X7R	10%	4000	148.36
748-5068	08052R472K9BB0	4700	50 V	X7R	10%	4000	170.62
748-5070	08052R103K9BB0	10000	50 V	X7R	10%	4000	152.07
748-5072	08052R473M8BB0	47000	25 V	X7R	20%	4000	192.87
748-5074	08052R104M8BB0	100000	25 V	X7R	20%	2000	111.27
748-5076	1206CG220J9BB0	22	50 V	C0G	5%	4000	152.07
748-5078	1206CG270J9BB0	27	50 V	C0G	5%	4000	218.84
748-5080	1206CG330J9BB0	33	50 V	C0G	5%	4000	152.07
748-5082	1206CG470J9BB0	47	50 V	C0G	5%	4000	152.07
748-5084	1206CG101J9BB0	100	50 V	C0G	5%	4000	152.07
748-5086	1206CG221J9BB0	220	50 V	C0G	5%	4000	152.07
748-5088	1206CG331J9BB0	330	50 V	C0G	5%	4000	189.16
748-5090	1206CG471J9BB0	470	50 V	C0G	5%	4000	189.16
748-5092	1206CG102J9BB0	1000	50 V	C0G	5%	4000	204.00
748-5094	1206CG222J9BB0	2200	50 V	C0G	5%	3000	300.44
748-5096	12062R102K9BB0	1000	50 V	X7R	10%	4000	178.04
748-5098	12062R103K9BB0	10000	50 V	X7R	10%	4000	152.07
748-5100	12062R473K9BB0	47000	50 V	X7R	10%	4000	204.00
748-5102	12062R104K9BB0	100000	50 V	X7R	10%	4000	218.84
748-5104	12062E103M9BB0	10000	50 V	Z5U	20%	4000	152.07
748-5106	12062E473M9BB0	47000	50 V	Z5U	20%	4000	152.07
748-5108	12062E104M9BB0	100000	50 V	Z5U	20%	4000	152.07

Panasonic® NHE

Miniature Radial Lead Aluminum Electrolytic Capacitors

PANASONIC NHE CROSS REFERENCES:
Elna: RE3; **Marcon:** BSM; **Nichicon:** VT;
Rubycon: SSP; **UCC:** KME.





Size Code	Dimensions (mm) D x L x A x d
A	5 x 11 x 2.0 x 0.5
B	6.3 x 11.2 x 2.5 x 0.5
C	8 x 11.5 x 3.5 x 0.6
D	8 x 12.5 x 3.5 x 0.6
E	10 x 12.5 x 5.0 x 0.6
F	10 x 16 x 5.0 x 0.6
G	10 x 20 x 5.0 x 0.6
H	12.5 x 20 x 5.0 x 0.6
I	12.5 x 25 x 5.0 x 0.6
J	16 x 25 x 7.5 x 0.8
K	16 x 31.5 x 7.5 x 0.8
L	18 x 35.5 x 7.5 x 0.8

Specifications:

NHE series has been introduced to meet the requirements of use of over wide temperature range of −55 ~ +105°C with same case size as SU series.

Features:

- Reduced case size, same as SU series
- 2,000 hours load life at 105°C
  (1,000 hours for products of 8mm dia. or less)
- Anti-solvent Freon TE, TES, TP-35
- Operating Temperature Range: −55 ~ +105°C
- Rated Working Voltage Range: 6.3 ~ 100V DC
- Rated Capacitance: 0.1 ~ 15,000μF
- Capacitance Tolerance: ±20% (at 20°C, 120 Hz)
- tan δ (at 20°C, 120 Hz)

W.V.	6.3	10	16	25	35	50	63	100
tan δ	0.28	0.22	0.19	0.16	0.13	0.10	0.09	0.07

Add 0.02 per 1,000μF for capacitors with more than 1,000μF.

- DC Leakage current:

I = 0.01 CV or 3μA, whichever is greater
where I = DC leakage current in μA
C = rated capacitance in μF
V = rated working voltage in V

DC leakage current shall be measured after 2 minutes application of the DC rated working voltage through the 1,000 ohms resistor at 20°C

- Load life:

After following load life test with DC voltage and ripple current applied (the sum of DC and ripple peak voltage shall not exceed the rated voltage), the capacitors shall meet following limits.

ϕ5, ϕ6, ϕ8 .... 1,000 hours at +105°C
ϕ10 ~ ϕ22.4 .... 2,000 hours at +105°C

Measurement shall be performed after 2 hours exposure at room temperature.

Add 0.5 (−25°C) or 1.0 (−40°C, −50°C) per 1,000μF for capacitors with more than 1,000μF.

Capacitance change	Within ±20% of the initial measured value
tan δ	Less than 200% of the initial specified value
DC leakage current	Less than the initial specified value

- Shelf life:

After storage for 1,000 hours at +105°C with no voltage applied, the capacitors shall meet the following limits.

Capacitance change	Within ±20% of the initial measured value
tan δ	Less than 200% of the initial specified value
DC leakage current	Less than the initial specified value

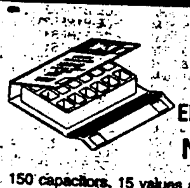
Measurement shall be performed after 2 hours exposure at room temperature.

- Stability at low temperature

Impedance ratio against value at +20°C, at 120 Hz.

W.V.	6.3	10	16	25	35	50	63	100
Z(−125°C)/Z(20°C)	4	3	2	2	2	2	2	2
Z(−40°C)/Z(20°C)	8	6	4	3	3	3	3	3
Z(−55°C)/Z(20°C)	12	10	8	6	6	6	6	6

Add 0.5 (-25°C) or 1.0 (-40°C, -50°) or 1,000 μF for capacitors with more than 1,000 pF.



Panasonic®
Miniature Radial Lead Aluminum Electrolytic Capacitors
NHE-Series Kit

150 capacitors, 15 values as denoted (*), 10 each. Price includes notebook style storage case and bin storage guide for convenient storage and quick access.

P5198-KIT-ND **$59.95**

[illegible]	μF	Case	Digi-Key	1	10	100	1,000	5,000	10,000	Panasonic #
6.3 (8)	47	A	P5202-ND	.25	1.85	16.02	74.00	70.00/M	64.00/M	ECE-A0JGE470
	100	A	P5203-ND	.27	2.03	17.55	81.00	77.00/M	70.00/M	ECE-A0JGE101
	220	B	P5204-ND	.33	2.48	21.45	99.00	94.00/M	86.00/M	ECE-A0JGE221
	330	B	P5205-ND	.34	2.51	21.78	100.00	95.00/M	87.00/M	ECE-A0JGE331
	470	D	[illegible]	.53	3.94	34.13	157.00	149.00/M	136.00/M	ECE-A0JGE471
	1,000	E	[illegible]	.74	5.55	48.10	222.00	210.00/M	192.00/M	ECE-A0JGE102
	2,200	H	[illegible]	1.09	9.36	73.32	468.00	443.00/M	405.00/M	ECE-A0JGE222
	3,300	H	[illegible]	1.11	9.54	74.73	477.00	451.00/M	413.00/M	ECE-A0JGE332
	4,700	J	[illegible]	1.74	14.91	116.80	745.00	705.00/M	645.00/M	ECE-A0JGE472
	6,800	J	[illegible]	1.85	15.87	124.32	793.00	750.00/M	687.00/M	ECE-A0JGE682
	10,000	K	[illegible]	2.36	20.25	158.63	1012.00	957.00/M	877.00/M	ECE-A0JGE103
	15,000	L	[illegible]	3.43	29.37	230.07	1468.00	1389.00/M	1217.00/M	ECE-A0JGE153
10 (13)	22	A	P5214-ND	.24	1.81	15.65	72.00	68.00/M	63.00/M	ECE-A1AGE220
	33	A	[illegible]	.25	1.85	16.02	74.00	70.00/M	64.00/M	ECE-A1AGE330
	47	A	[illegible]	.25	1.85	16.02	74.00	70.00/M	64.00/M	ECE-A1AGE470
	100	A	[illegible]	.26	1.95	16.90	78.00	74.00/M	68.00/M	ECE-A1AGE101
	220	B	[illegible]	.33	2.48	21.45	99.00	94.00/M	86.00/M	ECE-A1AGE221
	330	C	[illegible]	.57	4.28	37.05	171.00	162.00/M	148.00/M	ECE-A1AGE331
	470	D	[illegible]	.56	4.16	36.08	166.00	157.00/M	144.00/M	ECE-A1AGE471
	1,000	F	[illegible]	.83	6.23	53.95	249.00	235.00/M	216.00/M	ECE-A1AGE102
	2,200	H	[illegible]	1.09	9.33	73.09	466.00	441.00/M	404.00/M	ECE-A1AGE222
	3,300	I	[illegible]	1.26	10.83	84.84	541.00	512.00/M	469.00/M	ECE-A1AGE332
	4,700	J	[illegible]	1.82	15.60	122.20	780.00	738.00/M	675.00/M	ECE-A1AGE472
	6,800	K	[illegible]	2.29	19.62	153.69	980.00	928.00/M	849.00/M	ECE-A1AGE682
	10,000	L	[illegible]	3.19	27.36	214.32	1367.00	1294.00/M	1184.00/M	ECE-A1AGE103
16 (20)	10	A	[illegible]	.24	1.81	15.65	72.00	68.00/M	63.00/M	ECE-A1CGE100
	22	A	[illegible]	.24	1.81	15.65	72.00	68.00/M	63.00/M	ECE-A1CGE220
	33	A	[illegible]	.25	1.85	16.02	74.00	70.00/M	64.00/M	ECE-A1CGE330
	47	A	[illegible]	.25	1.88	16.25	75.00	71.00/M	65.00/M	ECE-A1CGE470
	100	B	[illegible]	.32	2.36	20.48	94.00	89.00/M	82.00/M	ECE-A1CGE101
	220	C	[illegible]	.57	4.28	37.05	171.00	162.00/M	148.00/M	ECE-A1CGE221
	330	D	[illegible]	.65	4.88	42.25	195.00	184.00/M	169.00/M	ECE-A1CGE331
	470	E	[illegible]	.74	5.55	48.10	222.00	210.00/M	192.00/M	ECE-A1CGE471
	1,000	G	[illegible]	1.02	7.61	65.98	304.00	288.00/M	264.00/M	ECE-A1CGE102
	2,200	I	[illegible]	1.27	10.89	85.31	544.00	515.00/M	471.00/M	ECE-A1CGE222
	3,300	J	[illegible]	1.81	15.51	121.50	775.00	733.00/M	671.00/M	ECE-A1CGE332
	4,700	K	[illegible]	2.31	19.80	155.10	989.00	936.00/M	857.00/M	ECE-A1CGE472
	6,800	L	[illegible]	3.21	27.48	215.26	1373.00	1299.00/M	1190.00/M	ECE-A1CGE682
25 (32)	10	A	[illegible]	.24	1.81	15.65	72.00	68.00/M	63.00/M	ECE-A1EGE100
	22	A	[illegible]	.25	1.85	16.02	74.00	70.00/M	64.00/M	ECE-A1EGE220
	33	A	[illegible]	.26	1.93	16.74	77.00	73.00/M	67.00/M	ECE-A1EGE330
	47	A	[illegible]	.26	1.95	16.90	78.00	74.00/M	68.00/M	ECE-A1EGE470
	100	B	[illegible]	.34	2.51	21.78	100.00	95.00/M	87.00/M	ECE-A1EGE101
	220	D	[illegible]	.62	4.65	40.30	186.00	176.00/M	161.00/M	ECE-A1EGE221
	330	E	[illegible]	.74	5.55	48.10	222.00	210.00/M	192.00/M	ECE-A1EGE331
	470	F	[illegible]	.87	6.53	56.55	261.00	247.00/M	226.00/M	ECE-A1EGE471
	1,000	H	[illegible]	1.10	9.42	73.79	471.00	445.00/M	408.00/M	ECE-A1EGE102
	2,200	J	[illegible]	1.85	15.84	124.08	792.00	749.00/M	686.00/M	ECE-A1EGE222
	3,300	K	[illegible]	2.36	20.22	158.39	1010.00	956.00/M	875.00/M	ECE-A1EGE332
	4,700	L	[illegible]	3.40	29.13	228.19	1456.00	1377.00/M	1261.00/M	ECE-A1EGE472
35 (44)	4.7	A	[illegible]	.24	1.81	15.65	72.00	68.00/M	63.00/M	ECE-A1VGE4R7
	10	A	[illegible]	.25	1.85	16.02	74.00	70.00/M	64.00/M	ECE-A1VGE100
	22	A	[illegible]	.26	1.93	16.74	77.00	73.00/M	67.00/M	ECE-A1VGE220
	33	A	[illegible]	.26	1.95	16.90	78.00	74.00/M	68.00/M	ECE-A1VGE330
	47	B	[illegible]	.33	2.48	21.45	99.00	94.00/M	86.00/M	ECE-A1VGE470
	100	C	[illegible]	.57	4.28	37.05	171.00	162.00/M	148.00/M	ECE-A1VGE101
	220	E	[illegible]	.75	5.59	48.43	223.00	211.00/M	194.00/M	ECE-A1VGE221
	330	F	[illegible]	.84	6.30	54.60	252.00	238.00/M	218.00/M	ECE-A1VGE331
	470	G	[illegible]	.99	7.43	64.35	297.00	281.00/M	257.00/M	ECE-A1VGE471
	1,000	I	[illegible]	1.28	11.01	86.25	550.00	521.00/M	477.00/M	ECE-A1VGE102
	2,200	K	[illegible]	2.39	20.49	160.51	1024.00	969.00/M	887.00/M	ECE-A1VGE222
	3,300	L	[illegible]	3.41	29.22	228.89	1460.00	1382.00/M	1265.00/M	ECE-A1VGE332
50 (63)	0.1	A	[illegible]	.24	1.80	15.60	72.00	68.00/M	62.00/M	ECE-A1HGE0R1
	0.22	A	[illegible]	.24	1.80	15.60	72.00	68.00/M	62.00/M	ECE-A1HGER22
	0.33	A	[illegible]	.24	1.78	15.28	70.00	67.00/M	61.00/M	ECE-A1HGER33
	0.47	A	[illegible]	.25	1.84	15.93	73.00	70.00/M	64.00/M	ECE-A1HGER47
	1.0	A	[illegible]	.24	1.80	15.60	72.00	68.00/M	62.00/M	ECE-A1HGE010
	2.2	A	[illegible]	.24	1.80	15.60	72.00	68.00/M	62.00/M	ECE-A1HGE2R2
	3.3	A	[illegible]	.24	1.80	15.60	72.00	68.00/M	62.00/M	ECE-A1HGE3R3
	4.7	A	[illegible]	.24	1.80	15.60	72.00	68.00/M	62.00/M	ECE-A1HGE4R7
	10	A	[illegible]	.24	1.80	15.60	72.00	68.00/M	62.00/M	ECE-A1HGE100
	22	A	[illegible]	.26	1.95	16.90	78.00	74.00/M	68.00/M	ECE-A1HGE220
	33	B	[illegible]	.34	2.55	22.10	102.00	96.00/M	88.00/M	ECE-A1HGE330
	47	B	[illegible]	.34	2.51	21.78	100.00	95.00/M	87.00/M	ECE-A1HGE470
	100	D	[illegible]	.63	4.69	40.63	187.00	177.00/M	162.00/M	ECE-A1HGE101
	220	F	[illegible]	.88	6.60	57.20	264.00	250.00/M	229.00/M	ECE-A1HGE221
	330	G	[illegible]	1.04	7.80	67.60	312.00	295.00/M	270.00/M	ECE-A1HGE331
	470	H	[illegible]	1.14	9.81	76.85	490.00	464.00/M	425.00/M	ECE-A1HGE471
	1,000	J	[illegible]	1.90	16.26	127.37	813.00	769.00/M	704.00/M	ECE-A1HGE102
	2,200	L	[illegible]	3.52	30.15	236.18	1507.00	1425.00/M	1305.00/M	ECE-A1HGE222
63 (79)	4.7	A	[illegible]	.25	1.85	16.02	74.00	70.00/M	64.00/M	ECE-A1JGE4R7
	10	A	[illegible]	.25	1.88	16.25	75.00	71.00/M	65.00/M	ECE-A1JGE100
	22	B	[illegible]	.32	2.40	20.80	96.00	91.00/M	83.00/M	ECE-A1JGE220
	33	B	[illegible]	.34	2.55	22.10	102.00	96.00/M	88.00/M	ECE-A1JGE330
	47	C	[illegible]	.61	4.58	39.65	183.00	173.00/M	158.00/M	ECE-A1JGE470
	100	E	[illegible]	.76	5.66	49.06	226.00	214.00/M	196.00/M	ECE-A1JGE101
	220	G	[illegible]	1.05	7.84	67.93	313.00	296.00/M	271.00/M	ECE-A1JGE221
	330	H	[illegible]	1.21	10.35	81.08	517.00	489.00/M	448.00/M	ECE-A1JGE331
	470	I	[illegible]	1.31	11.22	87.89	561.00	530.00/M	486.00/M	ECE-A1JGE471
	1,000	K	[illegible]	2.47	21.21	166.15	1060.00	1003.00/M	918.00/M	ECE-A1JGE102
100 (125)	0.47	A	[illegible]	.25	1.84	15.93	73.00	70.00/M	64.00/M	ECE-A2AGER47
	1.0	A	[illegible]	.24	1.80	15.60	72.00	68.00/M	62.00/M	ECE-A2AGE010
	2.2	A	[illegible]	.25	1.88	16.25	75.00	71.00/M	65.00/M	ECE-A2AGE2R2
	3.3	A	[illegible]	.25	1.88	16.25	75.00	71.00/M	65.00/M	ECE-A2AGE3R3
	4.7	A	[illegible]	.26	1.95	16.90	78.00	74.00/M	68.00/M	ECE-A2AGE4R7
	10	B	[illegible]	.34	2.51	21.78	100.00	95.00/M	87.00/M	ECE-A2AGE100
	22	C	[illegible]	.56	4.20	36.40	168.00	159.00/M	145.00/M	ECE-A2AGE220
	33	E	[illegible]	.73	5.48	47.45	219.00	207.00/M	190.00/M	ECE-A2AGE330
	47	F	[illegible]	.83	6.19	53.63	247.00	234.00/M	214.00/M	ECE-A2AGE470
	100	H	[illegible]	1.09	9.30	72.85	465.00	440.00/M	403.00/M	ECE-A2AGE101
	220	J	[illegible]	1.83	15.66	122.67	783.00	740.00/M	678.00/M	ECE-A2AGE221
	330	J	[illegible]	2.05	17.61	137.95	880.00	833.00/M	762.00/M	ECE-A2AGE331
	470	K	[illegible]	2.63	22.56	176.72	1127.00	1067.00/M	977.00/M	ECE-A2AGE471

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